23rd IMEKO TC4 International Symposium
Electrical & Electronic Measurements Promote Industry 4.0
September 17-20, 2019，Xi'an, China

DAC testing: recent research directions

E. Balestrieri, P. Daponte, L. De Vito, F. Picariello, S. Rapuano, I. Tudosa

Department of Engineering, University of Sannio
Benevento, Italy
{balestrieri, daponte, devito, fpicariello, rapuano, ioan.tudosa}@unisannio.it

***Abstract* – Digital to Analog Converters (DACs) represent essential components in many applications. During the years, their performances have been improved hand in hand with the increasing need to accurately test them. Due to the large number of different DAC applications, several different specifications have been used to quantify the effective performance of these converters in a particular context. To unambiguously clarify DAC terms, definitions and test methods the IEEE Std. 1658 has been developed and is currently under revision. The paper presents an overview of the last research work dealing with the DAC testing to highlight the trends and issues and provide useful information for the standard revision.**

***Keywords* –DAC, test, settling time, linearity, IEEE Std. 1658 standard, nonlinearity, uncertainty**

I. INTRODUCTION

Digital to Analog Converters (DACs) perform the function of transforming a digital signal into an analog signal. They are used by a very wide range of applications, including display electronics, motor control, software defined radio, data acquisition systems and test/measurement equipment. Due to their critical role, it is essential that DAC performance meets the specific application requirements that in the years have become more stringent and have also lead to the development of new converter architectures and techniques. As a consequence of the variety of the requirements, underlying conditions and different DAC architectures, it can be a challenge to correctly assess and compare DAC specifications.

To clear up confusion related to DAC terms and definitions, as well as to provide DAC terminology and test methods the IEEE Std. 1658 has been published in 2012 [1] and is currently under revision. Previous work has been already developed in the past on the DAC testing research directions [2]. However, during these last years, DAC architectures and application contexts have been subject of a continuous and fast evolving, introducing new challenges and points of interest, that have also led to the need of updating the IEEE Standard. To provide useful information in the standard updating process, this paper presents a review of the latest research on DAC testing. The main aim of the paper is to highlight prevailing issues and needs in the field, that can be considered in the revision of IEEE Std. 1658.

II. DAC RESEARCH TRENDS

Much of the scientific literature addressed to data converters continues to be devoted to Analog to Digital Converters (ADCs). An idea of the gap existing between the number of ADC and DAC research contributes is given in [3]: "*ADC papers in the circuits' conferences often outnumber the DAC papers by 3:1 or more*".

Concerning DAC research, last contributions are mainly focused on architecture design topics to optimize performance according to the different application requirements. Many design strategy techniques have been developed to deal with the DAC error sources [4], as for example DAC modelling [5-7] and calibration [8-10]. Fewer scientific works can be found focusing instead on DAC testing.

The topics addressed by the researchers in this field concerning the DAC static testing are mainly devoted to the reduction of the test time and cost also by means of the development of efficient DAC Built-In Self-Test (BIST) solutions operating in System on Chip (SoC) and System in Package (SiP) environments. Regarding, instead, the DAC dynamic testing, the research has been directed to the overcoming of the difficulties met in the characterization of some specific DAC parameters. Other research work has been focused on the lack of measurement uncertainty estimation procedures.

In the following subsections some research contributions belonging to the quoted above DAC testing topics are briefly presented.

A. DAC static testing

With the increasing demand for high performing DACs along with increasing resolutions, the required DAC testing time increases exponentially hand in hand with the test cost. This is especially true in the case of DAC static linearity testing, since it traditionally requires

a long time and is very expensive.

The testing method and algorithm introduced in [11] propose a solution for accurate DAC linearity testing with reduced test time and cost. In particular, the proposed algorithm comes from the consideration that the number of independent error sources is in most cases much smaller than the number of DAC codes examined in the linearity test. Thanks to that, it is possible to carry out linearity testing with much fewer samples saving on test time. In particular, the number of unknowns to be evaluated is decreased in [11] by means of a segmented non-parametric model for the INL curve of the DAC.
Moreover, the proposed method involves the use of an on-board digitizer for DAC output measurement in the place of a high accuracy digital voltmeter, resulting in less test time per sample. This test time reduction has the direct consequence of reducing the test cost, too. Additionally, the measurement error introduced due to the on-board digitizer is removed in the proposed algorithm, relaxing the stringent linearity requirement on the measurement device, allowing it to be orders of magnitude less linear than the DAC under test, implying further cost savings. The proposed method can be applied to DAC architectures inherently segmented, as binary weighted, R-2R and mDAC, but it is not valid for string or thermometer-coded type architectures [11].

Other proposals to overcome the requirements of high performance test equipment and at the same time to avoid the direct transfer of analog signal to external instruments are based on BIST approaches.

An example is the low speed BIST scheme for testing DAC static parameters presented in [12]. The proposed approach is based on an under-sampling technique. The DAC analog signal is modulated by the two sinusoidal carriers and then converted into low speed pulse stream. The relationship between nonlinearity of DAC and width of pulse stream can be further derived. Moreover, the required operational frequency of test equipment used in the proposed scheme is much lower than that of DAC [12]. In Fig. 1, the scheme of the proposed method along with the signals involved are shown. In particular, the BIST approach relies on the use of a sinusoidal carrier generator, two comparators, a logic control unit, a time to digital converter (TDC) and an all-pass filter acted as a delay element. The all-pass filter provides the sinusoidal carrier with a phase delay t_d, (Fig. 1.b). The comparators modulate the DAC output signal by both carriers resulting in narrow phase difference between two digital streams that represent the nonlinearity variation of DAC output signal. The logic unit provides the two digital stream phase difference and the TDC converts these pulse widths into readable binary codes. In Fig.1.c and Fig.1.d the shadow area of Fig.1.b is enlarged to show respectively the linear and the non-linear cases. Thanks to the very short duration between adjacent sample points, the sinusoidal carrier can be treated as the combination of piece-wise linear segments. As shown in Fig.1.d, in presence of non-linearities, the displacement of cross point of carrier and DAC output signal appears on the phase difference Δw. The method has been validated on 8-bits 200MS/s DAC, it could be interesting investigating the results obtained on DACs with greater resolution and speed.

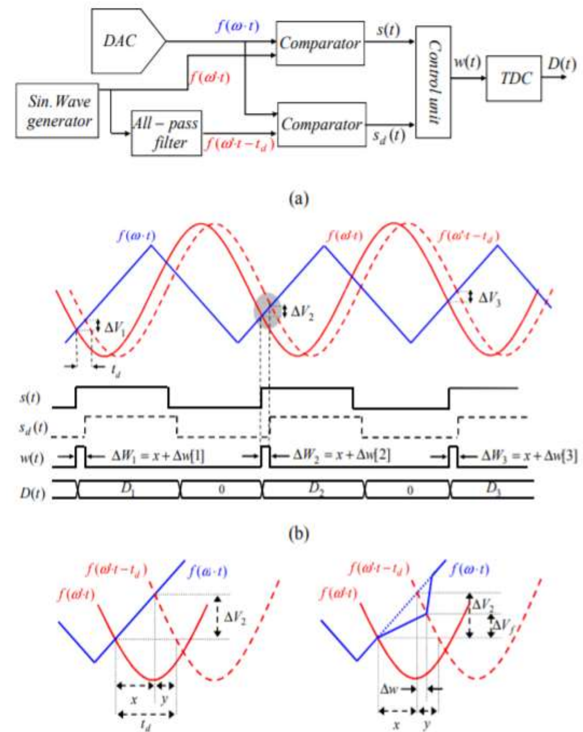

Fig. 1 a) The scheme of the proposed method with dual undersampling technique. b) The relative signals. c) The shadow area in Fig. 1(b) of linear case. d) The shadow area in Fig. 1(b) of non-linear case [12].

The BIST structure for data converter static testing proposed in [13] focuses on the frequent case in which an ADC and DAC pair is embedded in a SoC. By testing both the ADC and DAC converters simultaneously, the resulting test time can be decreased compared to other BIST approaches (i.e. loopback test). Moreover, the hardware overhead is reduced compared to that of the standalone BIST by sharing additional BIST circuitry for testing the converters. In Fig. 2 the proposed BIST scheme is shown. In particular, a counter is used for transition detection in ADC testing and as a test pattern generator in DAC testing. The ramp generator is used as a test input generator for ADC testing and as a voltage reference for DAC testing. For ADC and DAC simultaneous testing, the timing of each test must be arranged to share the use of the counter and the ramp generator. The proposed method is applicable when the ADC and DAC use the same system clock and have the same 1 LSB length [13].

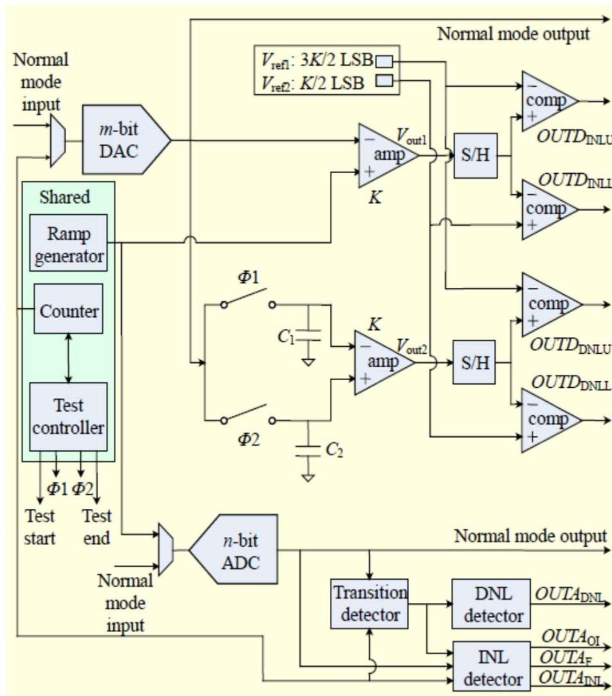

Fig. 2. BIST scheme proposed in [13].

B. DAC dynamic testing

DACs are currently used in a wide number of different applications, each having its own sensitivities to different specifications. As a consequence, research work about DAC testing can be focused on a particular specification of interest.

Settling time of the output signal is one of the most important parameters characterizing high speed DACs. However, it is also a challenging parameter to test accurately.

A method aimed at measuring in an automatic way the settling time of high-speed DACs with a mid-high resolution has been proposed and experimentally investigated in [14-16]. In particular, in order to perform automatic measurement of settling times of 12 or more bit DACs, the DAC output signal is converted to digital form and a digital signal processing is performed [14,15].
The algorithms proposed in [14,15] show the possibility of measuring the settling time of the high-speed DACs up to 16-bit resolution [16]. Moreover, by using those algorithms, it is possible to reduce the level of 1/f and white noise by 100 times without distorting the measurement signal itself.

Another relevant specification for high-speed high-accuracy DACs is represented by glitches. The DAC glitches, in fact, can compromise the overall converter spectral performance making it not suitable for specific applications. Unfortunately, different definitions and test methods exist making misinterpretations of the real DAC performance possible.

An experimental analysis of different DAC glitch definitions and measurement methods proposed in literature and adopted by manufacturers has been provided in [17]. In particular, the experimental investigation about the reproducibility of the results that can be achieved on the DAC varying the definitions and the test methods has been focused on (i) the applicability of each glitch definition and test method; (ii) the required computational complexity; and (iii) the possibility of automating the area measurement procedure excluding the need of the operator supervision. First results have shown that the restriction of the oscilloscope bandwidth greatly influences the estimation of glitch values. The analysis of the numerical integration methods that can be applied to compute the glitch has been focused on the rectangle methods (right and left corner, maximum and minimum corner and the midpoint), the trapezoid and Simpson's methods, as shown in Fig. 3. This analysis has highlighted also in this case the influence of the noise on the results. Moreover, the number of samples considered for the numerical integration greatly affects the goodness of results representing a critical problem since in case of very small and fast glitch only few samples can be caught. Further research work is needed to compare different definitions and testing procedures for DAC glitch by analysing different converters as well as to investigate the glitch waveform dependence from the used measurement equipment [17].

C. Measurement uncertainty

Currently, the evaluation of the measurement uncertainty is not yet included in any DAC standard. The measurement uncertainty is a quantitative indication of the quality of measurement and is essential to allow the comparison of results coming from different sources or with reference values given in specifications or standards.

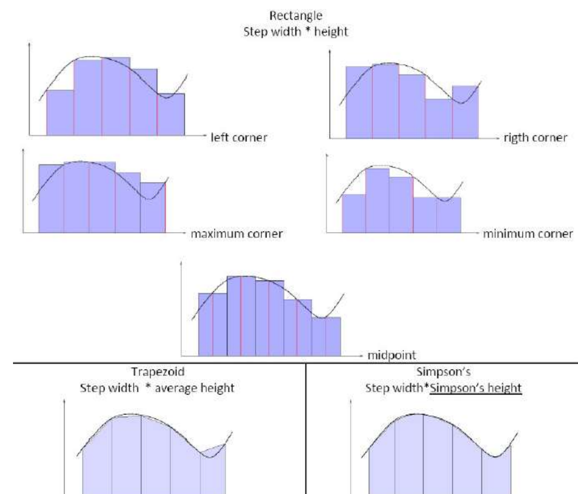

Fig. 3. Numerical integration methods analyzed in [17].

Although in the case of ADC research works dealing with the measurement uncertainty have been developed [18-22], the same was not found for DACs. Very few papers have been published in this field.

An example can be found in [23] where the evaluation of measurement uncertainty of time domain dynamic parameters as the DAC rise time and fall time relying on a bootstrap technique according to the “Guide to the expression of uncertainty in measurement” [24] has been presented. The proposed approach allows to define confidence intervals from short acquisition records without needing hypotheses about the measurand distribution, in an easy and fast way that can be interesting to make the method applied in the industrial environment. However, since the approach deals only with rise time and fall time, it would be useful to extend its application to other DAC parameters.

A new DAC testing method together with its analysis from the uncertainty point of view is provided in [25,26]. The test is based on the comparison of a time varying saw tooth signal generated by the converter under test with a reference signal by a fast comparator. The reference signal is the superposition of DC voltage measured by a precise DC voltmeter and slow dithering voltage with known amplitude. The comparator detects the sequence of DAC control codes which determines the DAC nonlinearities. The proposed method has been validated both by simulations and experiments on real setup under different working conditions. In Fig. 4, the simulation of the combined dependence of the uncertainty on record length (M) as well as on amplitude of dithering (W) is shown. Simulation results assess that the most important uncertainty factor is the number of samples and it influences the dithering amplitude W.

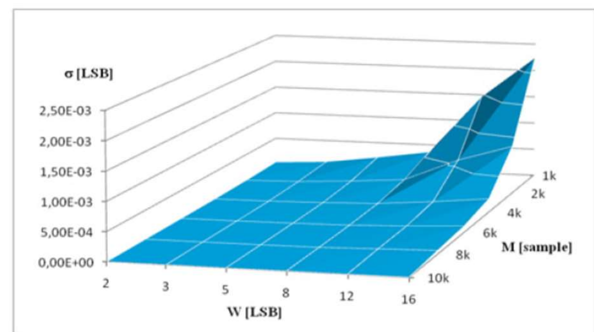

Fig. 4. Dependence of standard deviation of difference between INL characteristics on amplitude of dithering W and different record length M [25].

III. CONCLUSIONS

DACs today are used in an extremely large and growing number of applications in continuous and rapid evolution. Each application has its own performance requirements that the DAC has to meet. Data converter design and testing are strictly related to their reference application stringent performance specifications as well as driven by the technology advances.

Most of research in the field is focused on DAC architecture design strategies aimed at reaching the best performance in the specific application context. Fewer research contributions can be found concerning DAC testing.

Last research directions in this particular field are mainly aimed at providing mostly static testing methods requiring reduced time and cost, also paying attention to the situation in which the DAC operates in a SoC or in a System in Package SiP.

Source of the research interest is also the testing of some specific dynamic parameters as settling time and glitch, due to the challenging measurement keeping the suitable accuracy of the first one for high speed DAC and the ambiguity in the developed definition and testing methods for the second one.

Unfortunately, measurement uncertainty evaluation turns out to be an overlooked argument for DAC testing. However, information about this parameter is essential to evaluate the effectiveness of the proposed DAC testing methods and to compare DAC specifications. There is still a lot of research to be done on this specific aspect.

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