



Design and characterisation of a stand-alone merging unit

Giuliano Cipolletta¹, Antonio Delle Femine¹, Daniele Gallo¹, Carmine Landi¹, Mario Luiso¹

¹ Dept. of Engineering, University of Campania "Luigi Vanvitelli", 81031 Aversa (CE), Italy

ABSTRACT

Merging Units (MUs) play a key role in enhancing the levels of security and the reliability of power systems, allowing for advanced remote diagnostics. Some of the benefits are a more efficient transmission of electricity and a better integration with renewable energy systems. In this article, an implementation of a Stand-Alone Merging Unit (SAMU), compliant with the IEC 61850-9-2 standard and based on a low-cost ARM microcontroller, is described. It acquires two signals, one voltage and one current, and it sends the samples over the ethernet connection. A high-resolution Analogue-to-Digital Converter (ADC), synchronised to the Universal Time Coordinated (UTC) through a Global Positioning System (GPS) disciplined oscillator, is used. The opportune insulation and conditioning stage have been designed. Several tests have been performed, varying amplitude, frequency, and phase of the input signals, in order to evaluate the metrological performance of the proposed SAMU and they are here discussed.

Section: RESEARCH PAPER

Keywords: power system measurement; power system diagnostics; stand-alone merging unit; time synchronisation; analogue-to-digital converter

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Corresponding author: A. Delle Femine, e-mail: antonio.dellefemine@unicampania.it

1. INTRODUCTION

In recent years in the electricity supply industry, there has been a growing awareness of the need to re-invent Europe's electricity networks in order to meet the demands of 21st-century customers. This justifies the growing interest in smart grids [1], [2], and it increases, in turn, the interest in smart substation development. According to [3], Merging Units (MUs) play a crucial role in the design of substation communication and automation systems. Substation automation, using the IEC 61850 suite of protocols, is an established reality for the purpose of enabling fast-acting protection and control application.

Digital Substations (DSs) are electrical substations where operations are managed between distributed Intelligent Electronic Devices (IEDs) at different levels of automation, interconnected by communication networks. For a reliable information exchange among devices at different levels, data accuracy is needed not only for amplitude but in time as well.

The Stand-Alone Merging Unit (SAMU) [4] acts as digital interface of the instrument transformers. It converts to digital the analogue input signals from instrument transformers (inductive or low power i.e. LPIT) and provides a time-coherent

combination of the current and voltage samples, which are used to create a data stream of Sampled Values (SVs). SVs are used for transmitting digitised instantaneous values of power system quantities, mainly primary voltages and currents of one or multiple phases, to protection relays and bay controllers through either ethernet or optical communication channels based on the IEC 61850-9-2 protocol.

IEC 61850-9-2 handles this publication of SVs over the ethernet, which are sent to microprocessor-based IED. The benefits of digital process buses include a reduced complexity of Current and Voltage Instrument Transformers' (CTs and VTs) secondary cabling and a simplified connection for centralised substation automation functions, such as recording disturbances and monitoring power quality.

The presented work is part of the EMPIR 17IND06 Future Grid II research project. One objective of this project is to develop metrological grade SAMUs and traceable time synchronisation techniques.

Special care has to be taken to have accurate time synchronisation between units. Multiple devices will have their local independent clock, which cannot be used as time reference for the published data. Otherwise, samples coming from

different devices are not suitable for reconstructing the power network state [5], [6].

Therefore, SVs need to be accurately time-stamped, providing synchronisation information to put in the relation data from different IEDs placed in different locations of the smart grid. For this reason, local clocks must be synchronised to each other via a universal source. The standard [7] states that to ensure the deterministic operation of critical functions in the automation system, a precise time distribution and clock synchronisation in electrical grids with an accuracy of 1 μ s must be used. The Precision Time Protocol (PTP) [8], a network-based time synchronisation standard that can achieve clock accuracy in the sub-microsecond range, is suggested as time distribution mechanism. Such a synchronisation method implies considerable efforts by microcontroller firmware to generate an Analogue-to-Digital Converter ADC clock phase locked to the absolute time. In fact, continuous calibration of the internal microcontroller clock must be performed, with a proper closed-loop digital control system that follow the reference imposed by the PTP input.

To avoid this computational overhead and to achieve higher synchronisation accuracy, the proposed SAMU instead makes use of a Global Positioning System (GPS) Disciplined Oscillator (GPSDO) that allows long-term stability and does not need firmware calibration; the long-term stability relies on the high accuracy of GPS caesium references. The adopted solution allows for synchronisation for each sample with a higher time resolution.

In the following, Section 2 describes the hardware implementation of the proposed SAMU, whereas Section 3 focuses on the embedded measurement firmware. Section 4 shows experimental results from the metrological characterisation. Finally, Section 5 draws the conclusions.

2. HARDWARE ARCHITECTURE

The block diagram of the proposed SAMU [9] is shown in Figure 1. Figure 1. Block diagram of the proposed SAMU. It is based on a microcontroller, opportunely interfaced with a GPSDO and an ADC with proper designed conditioning circuits. The various functional blocks are explained in the following subsections.

2.1. Timing circuits

The Connor-Winfield FTS125-CTV-010.0M was adopted as the GPSDO. It produces a 1 Pulse Per Second (PPS) signal from the GPS timing receiver and generates both a 10 MHz CMOS-level square wave and a 10 MHz sine wave output from a low-jitter Voltage Controlled Temperature Compensated Crystal Oscillator (VCTCXO). It accomplishes the task of keeping the

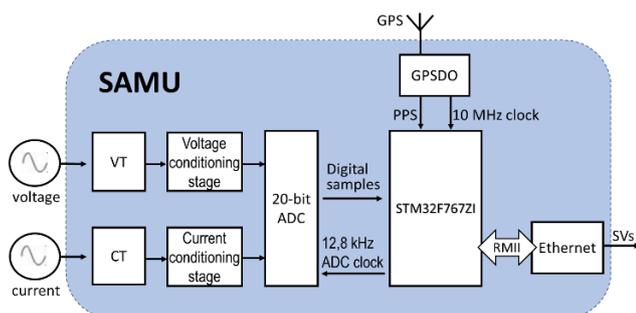


Figure 1. Block diagram of the proposed SAMU.

system synchronised to absolute time. In fact, it adjusts the frequency of the VCTCXO to be an integer multiple of the PPS and the relative phase, wherein the VCTCXO is adjusted to have 10 million oscillations in the PPS period, with the first pulse having the rising edge coincident with the PPS pulse.

2.2. Processing and coordination

The 10 MHz square wave is used as reference clock for the STM32F767ZI, an ARM-Cortex M7 microcontroller with 2 MB Flash, 512 kB of SRAM, a clock frequency of 216 MHz, a L1 cache, an Adaptive Real-Time (ART) accelerator, and a Digital Signal Processor (DSP) with a Floating Point Unit (FPU). The microcontroller is interfaced via Serial Peripheral Interfaces (SPI) with the external ADC MAX11960, which is a differential Successive Approximation Register (SAR) ADC with a resolution of 20 bits, a maximum sampling frequency of 1 MHz, a dual simultaneous sampling, a Signal-to-Noise Ratio (SNR) of 99 dB, Total Harmonic Distortion (THD) of -123 dB, and a differential non linearity of ± 1 LSB. The ADC has two independent SPIs with a shared clock, while the two SPIs of the microcontroller have two independent serial clock signals. Thus, in order to avoid electrical problems, one clock has been used for both channels.

2.3. Data acquisition stage

Data acquisition is performed in accordance with [3], using a sampling frequency of 12.8 kHz. Thus, the microcontroller supplies a 12.8 kHz sampling clock to the ADC in order to have 256 samples for each rated period of the fundamental component (i.e. 50 Hz).

The device has a differential ± 3 V input range, being the ADC reference voltage $V_{ref} = 3$ V. Thus, the signal conditioning stage produces a differential input signal centred around a common-mode DC voltage of $V_{ref}/2$.

A proper conditioning stage has been developed and it is presented in subsection 2.5. The conditioning circuits reproduce signals for voltage and current channels that lay within the operating range of the ADC. Once the signals are scaled down, accurately referred in time, they are sampled and converted to digital, and the microcontroller must transmit the SVs.

2.4. Communication

Regarding the communication hardware interface, STM32F767ZI features a 10/100 Mbit/s Ethernet Media Access Controller (EMAC) peripheral that consists of a MAC 802.3 controller. It complies with both the Media Independent Interface (MII) and the Reduced Media Independent Interface (RMII) to interact with the physical layer and supports ethernet frame time-stamping, as described in [8]. Furthermore, it has a dedicated Direct Memory Access (DMA) controller that interfaces with the core and memories through the Advanced High-Performance Bus (AHB) master and slave interfaces. The AHB master interface controls data transfers, while the AHB slave interface accesses the Control and Status Registers (CSRs) space. The Transmit First-In-First-Out (FIFO) buffers the data read from the system memory by the DMA, before the transmission by the Media Access Control (MAC). Similarly, the Receive FIFO stores the received ethernet frames until they are transferred to the system memory by the DMA.

2.5. Signal conditioning stage

In order to build up a complete SAMU, a voltage and current transducing stage has been realised. In Figure 2, an electric

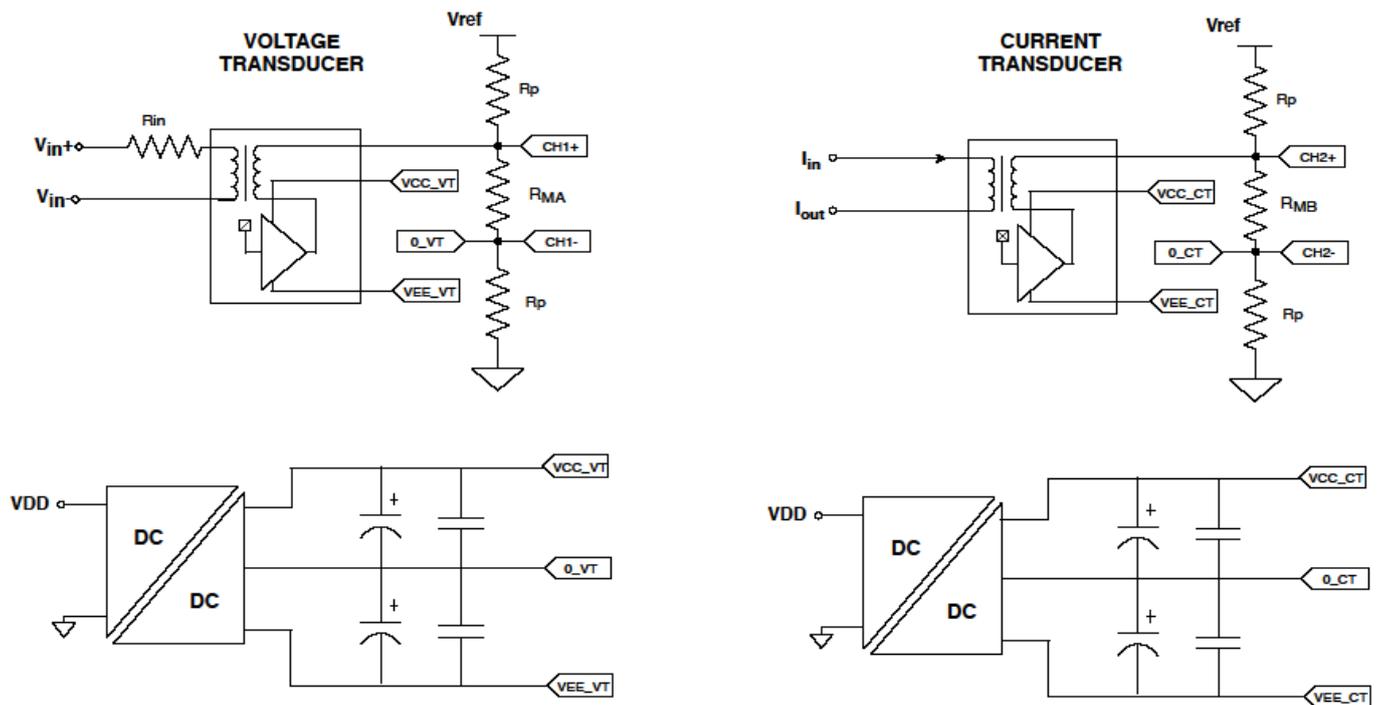


Figure 2. Voltage and current combined transducers.

scheme of the proposed combined transducer and conditioning section is shown.

The circuit fulfils two important tasks. The first is to guarantee electrical insulation in order to preserve the safety of workers and the integrity of instrumentations. The common-mode voltage between inputs of voltage transducers and the ground may be very dangerous. The second task is to adapt the signal levels and characteristics to the input of the digital conversion stage. The nominal input voltage and current of the proposed SAMU are 110 V and 5 A, root mean square (rms) value, respectively. These amplitude levels must be reduced to the range from -3 V to 3 V (i.e. the ADC input range). Moreover, the ADC works with fully differential inputs, so the signal must be converted from single ended to differential.

A magnetic insulation has been achieved by adopting, for both current and voltage channels, two zero-flux transformers. They consist of two commercial closed-loop compensated Hall-effect transducers, one for voltage and one for current channel. Obviously, the number of primary windings for the voltage transducer is higher than for the current. Moreover, for the voltage side, a primary resistor (R_{IN}) is needed and it is put in series in order to limit the primary current.

On the secondary of both voltage and current transducers, a passive network was used to maintain the highest possible linearity. Proper burden resistors (R_{MA} and R_{MB}) are chosen to tune the desired gain. The symmetric polarisation network obtained via identical R_P resistors is needed to obtain differential voltage signals from the current output of the two transducers.

Note that the two measurement transducers have independent power supply circuits, both insulated with respect to the main supply and, of course, with respect to the 0 V reference of the ADC. This is necessary in order to obtain differential signalling with the simple passive network. This network is supplied by the reference voltage V_{REF} of the ADC, and the current flow in the measurement resistor R_M produces a voltage drop, which is symmetrically split between $CH+$ and $CH-$

nodes with respect to the 0 V reference of the ADC, producing two equal signals with opposite phases.

It is important to highlight that all the adopted resistors consist of precision metal film-leaded resistors that have a very good overall stability, thanks to an extremely low Temperature Coefficient of Resistance (TCR) of $\pm 2\text{ ppm/K}$ and a very tight tolerance in the range of $\pm 0.01\%$ to $\pm 0.25\%$.

The passive resistive divider networks, obtained with the series R_P , R_M , and R_P , again produce an offset voltage for both channels equal to:

$$V_{\text{off}} = \frac{V_{\text{REF}} R_M}{2 R_P + R_M} \quad (1)$$

This offset voltage has been maintained as reasonably low, choosing R_P 2 order of magnitude higher than R_M . By calculating Equation (1), V_{off} becomes almost 0.5% of V_{REF} .

This offset and the other offset due to the transducer feedback amplifier have been measured and digitally compensated by means of microcontroller's firmware.

3. EMBEDDED MEASUREMENT FIRMWARE

The microcontroller was programmed using Standard C Language. The firmware implements the opportune drivers for all the described hardware devices and performs their coordination. Starting from the disciplined 10 MHz clock, the 12.8 kHz sampling has to be produced for the ADC.

There are various possible solutions for this problem. Most of them, however, involve firmware latency. The only one that completely avoids this issue is the use of the 10 MHz clock as the main oscillator for the entire microcontroller. In this way, all the internal clocks of the microcontroller are locked in frequency and phase with the absolute time, and it is possible to construct the time base for the ADC using only internal hardware devices, without involving execution time latency due to firmware routines. In particular, the time base for the ADC has been built

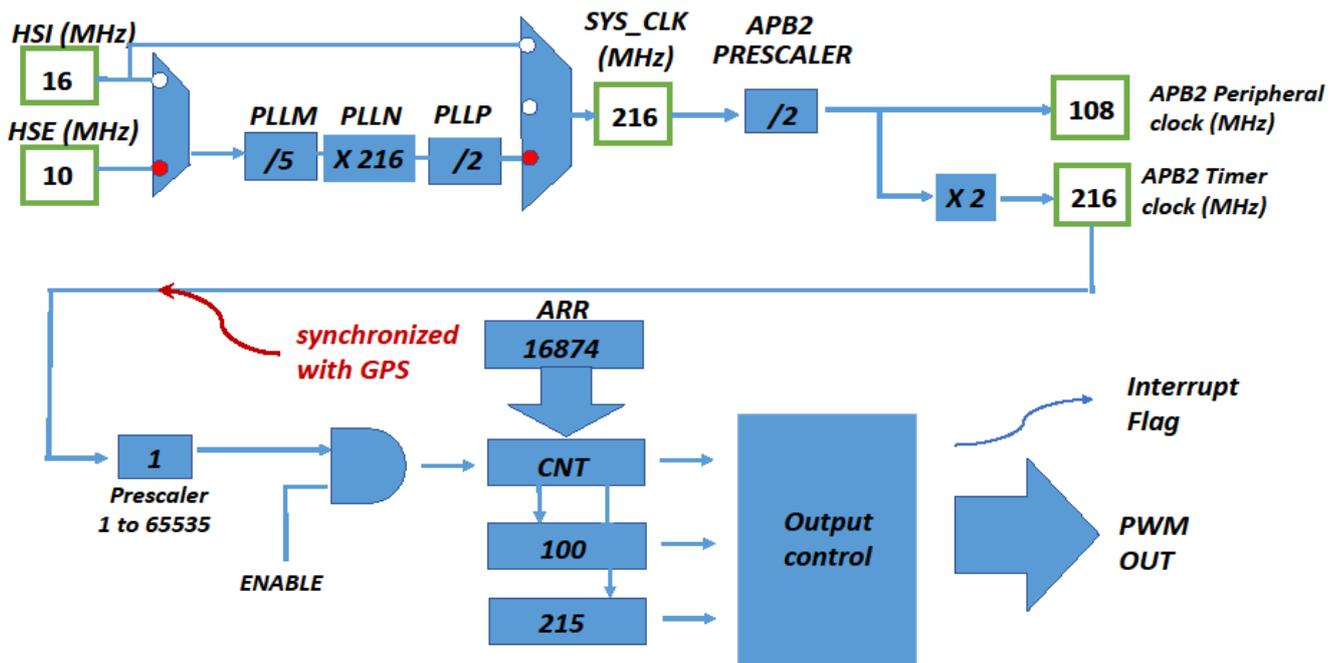


Figure 3. Clock configuration.

by making use of an internal timer as a key peripheral. In summary, the 10 MHz clock reference signal from GPSDO has been used as an external source and is given to the internal microcontroller Phase Locked Loop (PLL) circuit, which allows an increase in the frequency of up to 216 MHz. The timer peripheral acts as a divider, automatically controlling the external Pulse Width Modulation (PWM). This line is used to clock the ADC. To maintain a high level of accuracy, Interrupt Service Routines (ISRs) have been avoided, and the timer is configured to control the output in the hardware, without latency.

Figure 3 shows a block diagram of a sample clock generation. The system clock (SYS_{CLK}) is obtained by Equation (2) and is equal to 216 MHz:

$$SYS_{CLK} = \frac{HSE \cdot PLLM \cdot PLLN}{PLL P} \quad (2)$$

The timer accurately divides the system clock by 16875 in order to generate a 12.8 kHz square wave using the PWM output. The standard PWM mode is programmed with the Auto-Reload Register (ARR) and the Capture Compare Register (CCR) to define the period and the duty cycle respectively.

Note that two different timers have been used for the two different channels. Moreover, controlling the duty cycle and the polarity of the sample clock signal, it is possible to control the sampling instant position with respect to the 1-PPS signal. Consequently, it is possible to fine tune the absolute phase of the two channels within one sample range (i.e. $2 \cdot \pi / 256$ rad at the chosen sampling frequency at 50 Hz with a resolution of $2 \cdot \pi \cdot 50 / 216 \mu\text{rad}$, thanks to the timer frequency of 216 MHz).

As mentioned in Section 1, the aim of the presented work is to realise an accurate SAMU. According to [10], the requested accuracy for the highest time performance class (i.e. T5) must be $\pm 1 \mu\text{s}$. The use of GPSDO offers significant advantages in terms of synchronisation accuracy.

Moreover, the microcontroller firmware receives and parses National Marine Electronics Association (NMEA) sentences from the GPS receiver to obtain a time stamp. Since the SAMU must associate a time stamp with each sample, a hard real-time

mechanism has been implemented in order to identify the precise instant in which a one-second frame starts, using a PPS signal external interrupt. Obviously, this synchronisation is needed only on the first PPS frame at start up. From this moment on, the system proceeds to count up each sample time and follows the eventual corrections carried on by GPSDO. The firmware checks this correction process, monitoring the difference between internal counters (locked on disciplined 10 MHz from DO) and NMEA time strings (locked on PPS signal from GPS system). This difference must converge in the interval of ± 200 ns within a maximum time (which is used to detect time out condition).

The microcontroller is responsible for IEC61850-9-2 communication via ethernet as well. To fulfil this task, the integration between the Lightweight Internet Protocol (LwIP) stack and libiec61850 [11] (an open-source implementation of the standard) were realised. This integration was conducted through a Berkley Software Distribution (BSD) socket interface

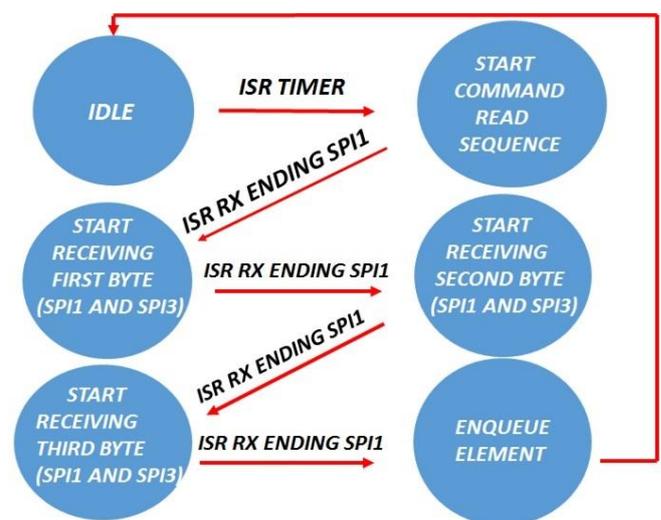


Figure 4. ADC samples collection via SPI.

in the LwIP stack. IEC 61850-9-2 is based on a RAW socket, not fully supported by LwIP. It was necessary to extend that support, opportunely modifying the whole library code.

A producer-consumer design pattern was chosen for the data acquisition from the external ADC. The samples reading is achieved by means of the event-based state machine shown in Figure 4. The transition between the states is interrupt-based. In this way, the microcontroller can perform other tasks, like sending the sample frames through the ethernet. Once the timer is enabled and started in PWM mode, a 12800 Hz square wave synchronised with GPS is produced and used as a conversion starter for both MAX11960 channels A and B in order to have a simultaneous sampling between the voltage and current signals. The rollover timer ISR was used to start the state machine; from this moment on, it evolves by interrupts from the Serial Peripheral Interface (SPI) used for data transfer from the ADC.

The microcontroller firmware has been used also to compensate all the systematic errors of the proposed SAMU. The gain and the offset of the whole measurement chain for both channels, measured during the metrological characterisation of the proposed instrument, have been compensated. Moreover, the absolute phase error of each channel was determined and compensated at 50 Hz, acting, as previously described, on the duty cycle of the PWM timer output, which tunes the sampling instant position with respect to the 1-PPS edge.

4. EXPERIMENTAL TEST

Several tests were conducted on the realised instrument in order to fully characterise its metrological performance. In the following subsections, the more relevant test setups with related experimental results are explained. In particular, the linearity of the system was evaluated by dynamic testing of the ADC, but the procedure also involved the whole chain, thus performing the tests at various amplitude levels. Synchronisation accuracy was evaluated by comparing a reference clock signal with the one produced by the adopted GPSDO, but it also involved the whole chain again, adopting a PMU calibration facility.

4.1. ADC dynamic test

The block diagram of the measurement setup for the ADC dynamic test is shown in Figure 5 [12].

In particular, the Effective Number Of Bit (ENOB) of the ADC was evaluated. The dynamic ADC test method requires a high spectral purity test signal. This special signal must have a distortion of at least 10 dB lower than that of the tested ADC. For a 20-bit ADC, a Signal to Noise And Distortion ratio (SINAD) of 120 dB is required. Moreover, the SAMU is a device that should measure signals at power frequency, so the frequency

of the test signal should be of 50/60 Hz. It is very difficult to achieve such spectral purity, particularly at a low frequency, because it is very difficult to build a good linear filter at low frequencies. For these reasons, the test was conducted at 1 kHz. For this test, with reference to Figure 5, a National Instruments PCI eXtension for Instrumentation (NI PXI) chassis, housing the NI-5422 (16 bit, ± 12 V, 200 MHz Arbitrary Waveform Generator, AWG) and the NI-5922 (24 bit, ± 5 V, 500 kHz Data Acquisition Board, DAQ), were used. The PXI chassis was provided with a 10 MHz external clock source from the GPSDO. Both boards have been configured to use the PXI clock as a reference clock in order to ensure coherent sampling between NI-5422, NI-5922, and the proposed reference SAMU under test.

A sinusoidal signal with an amplitude equal to the ADC input range and frequency of 1 kHz were used as the test signal and were directly supplied (excluding conditioning stages) to both the SAMU ADC and to the DAQ. In Figure 6, the magnitude spectrum of the signal generated by the AWG is reported, which reaches a SINAD of 76.7 dB.

Using the DAQ as a reference device, a closed-loop compensation was implemented in order to enhance the spectral purity of the test signal. The magnitude spectrum of the sine

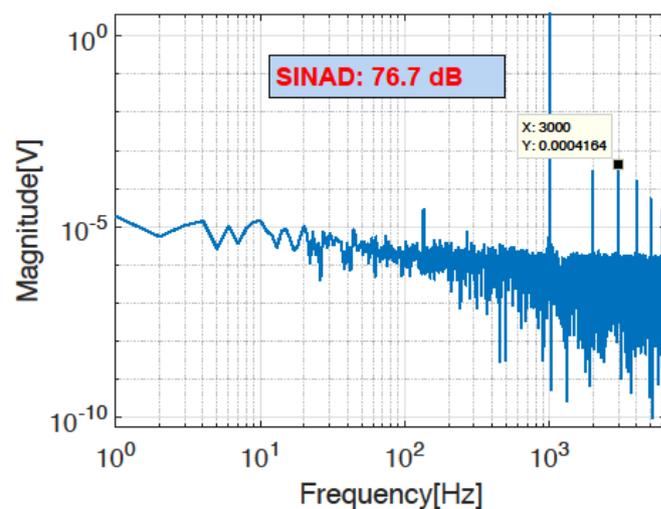


Figure 6. Magnitude spectrum of the test signal obtained with AWG only.

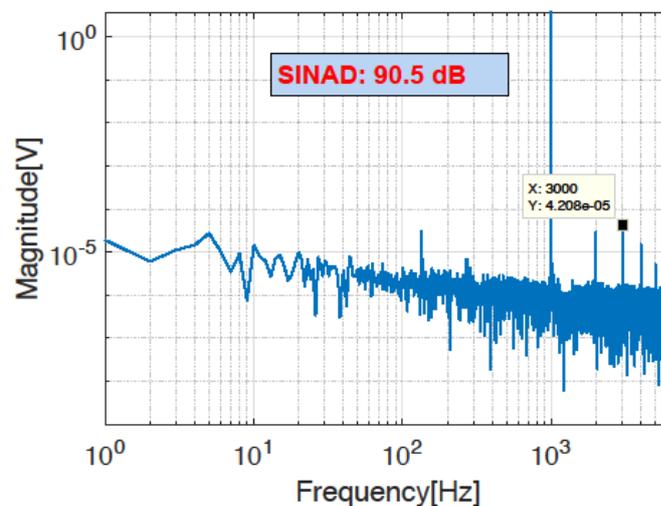


Figure 7. Magnitude spectrum of the compensated test signal.

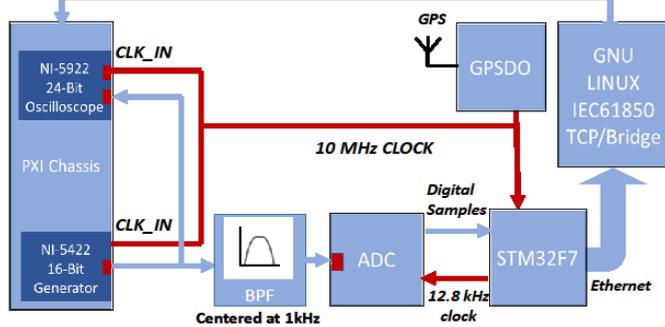


Figure 5. Dynamic ADC test setup.

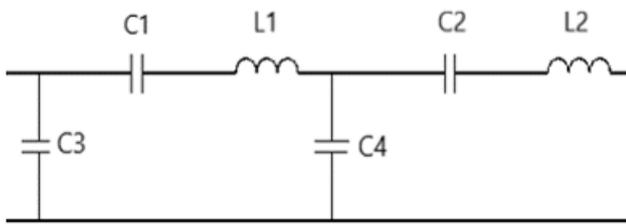


Figure 8. Electric scheme of the band pass resonant passive filter.

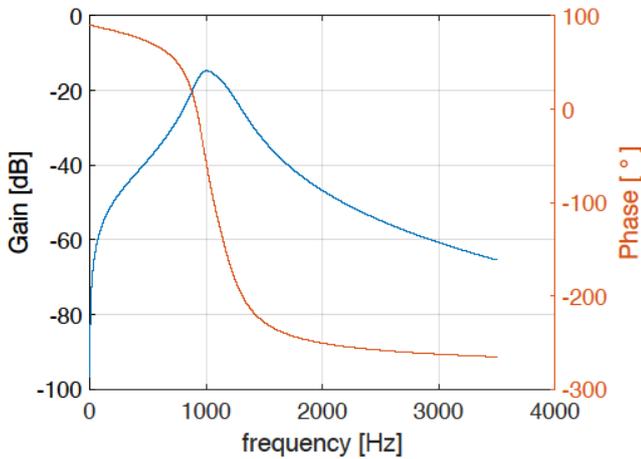


Figure 9. Magnitude and phase response of the filter.

wave obtained with this technique reported in Figure 7. Note that the amplitude of the harmonic components is reduced by an order of magnitude, and consequently, the SINAD increases to 90.5 dB. Nevertheless, as we mentioned before, this is not enough to test a 20-bit ADC. To further enhance the spectral purity of the signal, a passive linear filtering stage was added to the measurement setup. The electric scheme of the filter and its magnitude and phase frequency response are shown in Figure 8 and Figure 9, respectively. This is a narrow band-pass filter properly designed with a resonance frequency of 1 kHz and realised adopting only tantalum capacitors and air-cored inductors in order to fulfil the high linearity requirements [13].

Adopting both a compensation technique and analogue filtering to enhance spectral purity, a test signal with a SINAD of almost 104 dB (measured without the parallel connection of the SAMU ADC) has been obtained. Figure 12 shows the magnitude spectrum of this signal. Obviously, this is not enough, but it is quite good for the preliminary characterisation of the proposed SAMU with a design validation purpose. The software for the measuring setup was developed in LabVIEW on Windows Operating System (OS). Unfortunately, Windows has poor support for RAW sockets. For this reason, the measurement results, i.e. the sampled values of the SAMU, are sent via ethernet to an IEC 61850-9-2/TCP (Transmission Control Protocol) bridge (realised using [11]) and subsequently to the PXI controller.

However, when parallel connecting the SAMU ADC, the spectral purity deteriorates significantly. In fact, as depicted in Figure 10, which shows the magnitude spectrum of the SV, the spectral purity becomes lower as the SINAD drops to about 88.5 dB. It shows the presence of the same harmonics of the test signal, but there is an important presence of an undesired 50 Hz spectral component and its second harmonic (100 Hz) uncorrelated with the input signal. This presence, together with

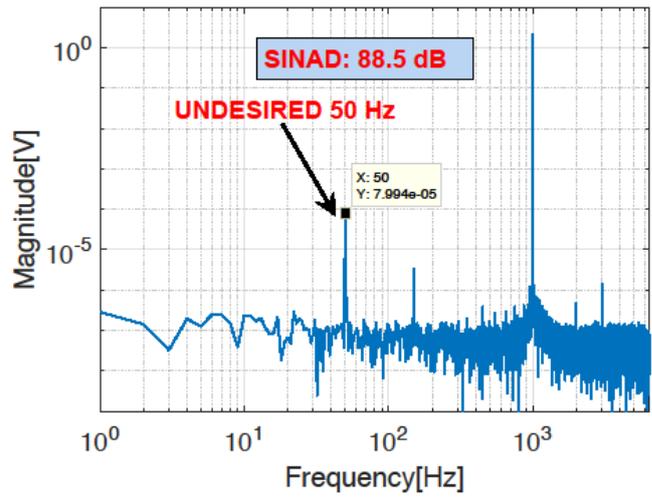


Figure 10. Magnitude spectrum of the sampled values.

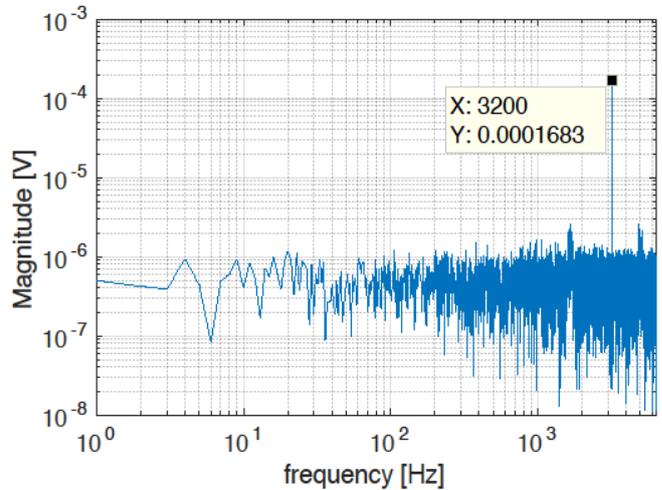


Figure 11. Magnitude spectrum of the sampled values with 0 V at the input of the ADC.

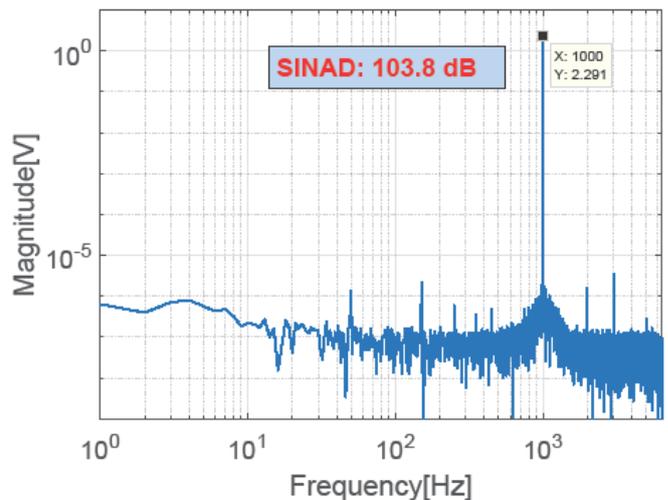


Figure 12. Magnitude spectrum of the test signal at the output of the filter.

a load effect that slightly reduces the amplitude of the test signal, makes the SINAD decrease. It is important to highlight that the noise floor of the SVs (Figure 10) is comparable to that which is obtained using the DAQ board (Figure 12).

Moreover, it is important to highlight that there is an undesired spectral component at exactly 3200 Hz, which is not present in the input signal. This spurious spectral component is uncorrelated with the input signal. To prove that consideration, another test has been conducted, putting zero volts at the input of the ADC (with a short circuit). As shown from Figure 11, the undesired tone is still present, located at the frequency $f_a = 3.2$ kHz. Investigations concerning this issue (changing the sampling frequency and/or changing the clock signal amplitude and frequency) led to the realisation that the disturbance is due to capacitive coupling with the 10 MHz clock signal. This last frequency is aliased according to Equation (3):

$$f_a = |f_{\text{clock}} \pm k \cdot f_s| \quad (3)$$

where f_{clock} is the clock signal at 10 MHz, and f_s is the sampling frequency of 12.8 kHz. Choosing $k = 781$ the f_a result exactly equals 3.2 kHz.

Despite its small amplitude, the spurious component is considerably higher than the noise floor. Further efforts to enhance the performance of the anti-aliasing filter at the input of the ADC are in progress. It is important to highlight that this problem is due to the choice of sampling frequency. By choosing a frequency submultiple of 10 MHz, the spectral component will fall at 0 Hz and could be compensated as a further contribution to the offset. However, the sampling frequency is not an arbitrary value; rather, it will be established by a future standard focused on SAMUs.

4.2. Synchronisation test

In order to evaluate the time synchronisation accuracy of the proposed SAMU, other experimental tests were conducted. An Agilent 53230A Universal Frequency Counter was used to determine the conversion starter stability. The experimental results show that a standard deviation of 10 μ Hz for the sampling frequency was obtained. Furthermore, the maximum error of the sampling period, measured over a 10-minute observation time, is about 200 ns [10].

Another test was conducted comparing the PPS signal from a reference clock to that coming from the adopted GPSDO. A Fluke 910R atomic clock, which exhibits a maximum jitter on the 1-PPS output (when locked to GPS) less than 60 ns relative to UTC, was used as a reference. Figure 13 shows the distribution of the delay between the 1-PPS signal from the GPSDO and that coming from the reference clock. The test duration was 960 s. The maximum error is lower than 200 ns and the mean is -5.4 ns.

4.3. Amplitude test

Other tests were conducted in order to evaluate the amplitude linearity and relative phase accuracy of the proposed SAMU. For these tests, a Fluke 6105A electrical power calibrator was used (see Figure 14) to generate a signal typical of power systems in sinusoidal conditions. For all the tests, 31 iterations (according with GUM [14]) having 2 s duration were carried out. The standard uncertainty was calculated for the 31 iterations and added quadratically to the uncertainty of type B of the calibrator in the corresponding amplitude range. The measurements' expanded uncertainty, with a coverage factor 3, are reported in the error bars of the subsequent figures. It is noteworthy that for the first test set, the voltage amplitude was varied in the range of 80 % to 120 % of the nominal value (110 V), and the current amplitude was varied in the range of 60 % to 120 % of the nominal value (5 A). The voltage rms, the current rms, and active power [15] were calculated for the acquired data, as shown in

Figure 15. The current has a dominant influence on the error in the measurements of active power. The ADC and the conditioning network are symmetric, so the simple conclusion is that to further enhance the performance of the SAMU, the current transducer must be enhanced.

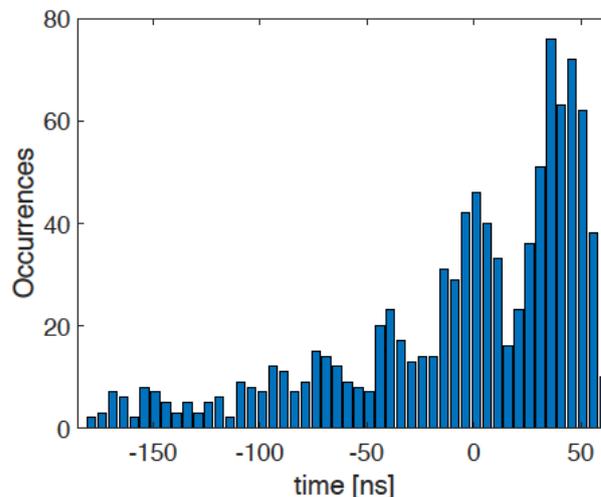


Figure 13. Distribution of the jitter on the 1-PPS output of GPSDO.

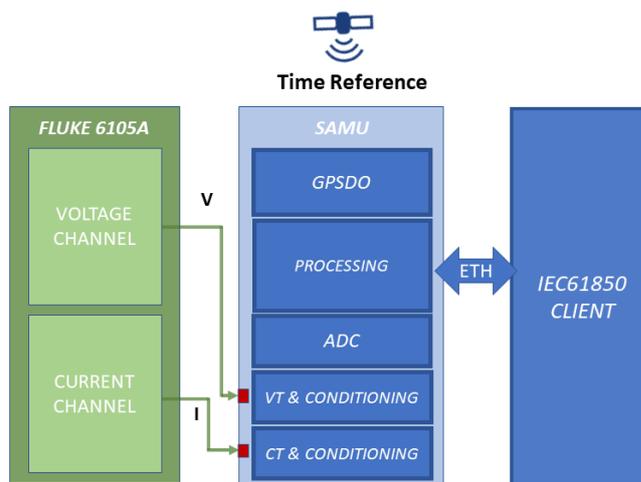


Figure 14. Amplitude test setup.

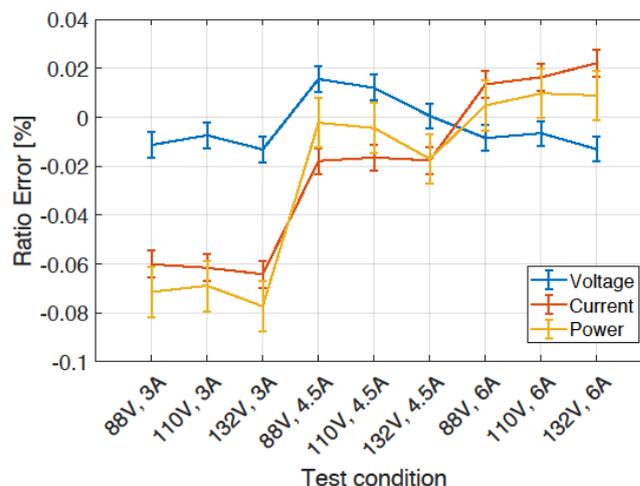


Figure 15. Ratio error on RMS Voltage, RMS Current and Active Power, varying the amplitude level.

4.4. Absolute phase test

Further experimental tests to evaluate the synchronisation error involving the whole measurement chain, from the transducers to the digital sampled values, were conducted by means of Fluke 6135A/PMU-CAL. Figure 16 shows the block diagram of the measurement setup. This special instrumentation has been designed for testing the Phasor Measurement Units (PMUs), instruments devoted to synchrophasor measurement [16]. To this end, PMU-CAL is a calibrator that can generate signals accurately, referenced in phase to the absolute time.

It exhibits a phase standard uncertainty of 32 μ rad. Taking advantage of this characteristic, it has been possible to evaluate the phase error of the proposed SAMU with reference to the absolute time in steady state conditions. In Figure 17, the absolute phase error of the proposed instrument for both the voltage and current are reported, varying the input frequency in the range of 45 Hz to 55 Hz. 31 iterations having a 2 s duration were also performed for these tests. The standard uncertainty (evaluated with type A method) was calculated for the 31 iterations and was quadratically added to the uncertainty contribution (type B method) of the PMU-CAL. The expanded combined uncertainty (level of confidence 99 %) is reported in the error bars. Note that the phase error is very small at 50 Hz as a result of the compensation of the systematic error obtained by time shifting the sampling instant with respect to absolute time. Of course, this kind of time domain compensation works very good only at one frequency. However, whereas the performance shown is quite good in the range of interest, it is noteworthy that almost all the measurements are compatible, which is due mainly to the uncertainty of the reference instrument.

5. CONCLUSIONS

This paper discussed the implementation of a reference SAMU based on an ARM microcontroller. It also included an external high-resolution ADC, a conditioning stage, a VT and a CT as well as a GPSDO. Great care was given to the realisation of the insulation and conditioning stages. Experimental results of the evaluation of the ENOB and the stability of the time base have also been presented. Some results coming from a comprehensive metrological characterisation have also been reported here. The system exhibits deviations lower than 0.02 %, 0.06 % and 0.08 %, respectively on voltage, current and power measurement.

The authors are currently working at two aspects of the realized SAMU: 1) improving the accuracy of the current channel, in order to reach the same accuracy exhibited by the voltage channel; 2) reducing the interferences, on the measured signals, induced by the capacitive coupling with the 10 MHz clock and other external radiated or conducted disturbances.

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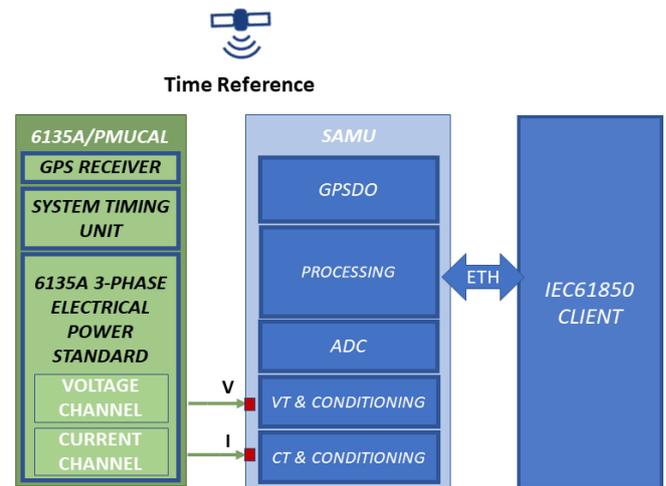


Figure 16. Absolute phase test setup.

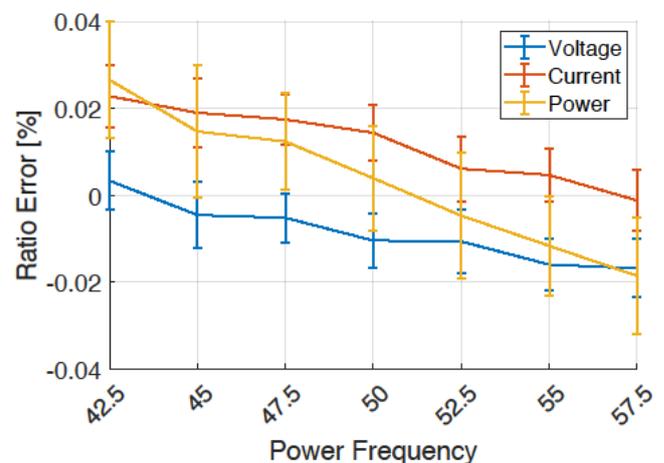


Figure 17. Absolute phase error in varying the power frequency.

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