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# Design Approach for a Stand Alone Merging Unit

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***Abstract* – In order to enhance levels of security and reliability of power systems, allowing for advanced remote diagnostics, Merging Units (MUs) play a key role. Some of the benefits are a more efficient transmission of electricity and a better integration with renewable energy systems. In this paper an implementation of a Stand Alone Merging Unit (SAMU), compliant with the IEC 61850-9-2 standard and based on a low cost ARM microcontroller, is described. It acquires two signals, one voltage and one current, and it sends the samples over the Ethernet connection. A high-resolution analog to digital converter (ADC), synchronized to the Universal Time coordinated (UTC) through a Global Positioning System (GPS) disciplined oscillator, is used. The results of the characterization of the ADC are presented.**

***Keywords* – *Power System Measurement, Power System Diagnostics, Stand Alone Merging Unit, Time Synchronization, Analog To Digital Converter.***

## I. INTRODUCTION

In recent years, within the electricity supply industry there has been a growing awareness of the need to reinvent Europe's electricity networks in order to meet the demand of 21st century customers. This justifies the growing interest in smart grids [1,2] and it increases, in turns, the interest in smart substation development. According to [3], Merging Units (MUs) play a crucial role in the design of substations communication and automation systems. Substation automation using the IEC 61850 suite of protocols is an established reality for the purpose of enabling fast-acting protection and control application.

The Digital Substations (DSs) are electrical substations where operations are managed between distributed Intelligent Electronic Devices (IEDs) at different levels of automation, interconnected by communication networks. For a reliable information exchange among devices at different levels, data accuracy is needed not only on amplitude but in time as well.

The Stand Alone Mering Unit (SAMU) [4] acts as digital interface of the instrument transformers. It converts to digital the analog input signals from instrument transformers (inductive or low power, i.e. LPIT) and provides a time-coherent combination of the current and voltage samples, which are used to create a data stream of Sampled Values (SVs). SVs are used for transmitting digitized instantaneous values of power system quantities, mainly primary voltages and currents of one or multiple phases, to protection relays (PRs) and bay controllers (BCs) through either Ethernet or optical communication channels based on the IEC 61850-9-2 protocol.

IEC 61850-9-2 handles this publication of SVs over the ethernet that are sent to microprocessor-based IED. The benefits of digital process buses include a reduced complexity of Current and Voltage Instrument Transformers (CT and VT) secondary cabling and a simplified connection for centralized substation automation functions such as the disturbances recording and the power quality monitoring.

The presented work is part of EMPIR 17IND06 Future Grid II research project: one objective of this project is to develop metrological grade Stand Alone Merging Units and traceable time synchronization techniques.

Special care has to be taken to have accurate time synchronization between units. Multiple devices will have their local independent clock which can not be used as time reference for the published data. Otherwise, samples coming from different devices are not suitable to reconstruct the power network state [5, 6].

Therefore SVs need to be accurately time stamped, providing synchronization information to put in relation data from different IED placed in different locations of the smart grid. For this reason Local clocks must be synchronized to each other via a universal source. The standard [7] states that, to ensure deterministic operation of critical functions in the automation system, a precise time distribution and clock synchronization in electrical grids with an accuracy of 1 $\mu$s must be used.

The Precision Time Protocol (PTP)[8], that is a network-based time synchronization standard that can achieve clock accuracy in the sub-microsecond range, is suggested as time distribution mechanism. Such a synchronization method implies considerable efforts by microcontroller firmware to generate an ADC clock phase locked to the absolute time. In fact, continuous calibration of the internal microcontroller clock must be performed, with a proper closed loop digital control system that follow the reference imposed by PTP input.

To avoid this computational overhead and to reach higher synchronization accuracy, the proposed SAMU, instead, makes use of a GPSDO (GPS Disciplined Oscillator), that allows a long term stability and does not need

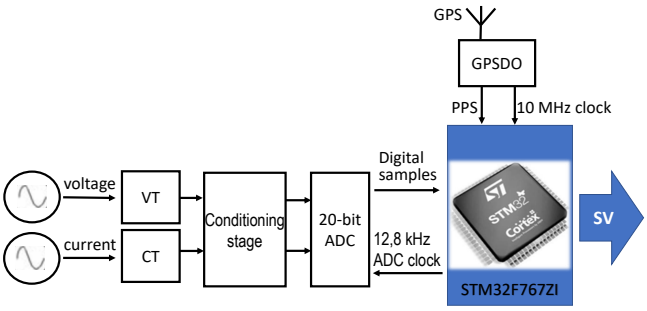


*Fig. 1. Block diagram of the proposed SAMU*

firmware calibration; the long term stability relies on the high accuracy of GPS Caesium references. The adopted solution allows to get synchronization on each sample with higher time resolution.

In the following, Section II describes the hardware implementation of the proposed SAMU, whereas Section III focuses on the embedded measurement firmware. Section IV shows experimental results of the ADC characterization. Finally, Section V draws the conclusions.

## II. HARDWARE ARCHITECTURE

The block diagram of the proposed SAMU is shown in Fig. 1. The Connor-Winfield FTS125-CTV-010.0M was adopted as GPSDO. It produces a 1-PPS (1 Pulse Per Second) signal from the GPS timing receiver and generates both a 10 MHz CMOS levels square wave and a 10 MHz sine wave output from a low jitter VCTCXO (Voltage Controlled Temperature Compensated Crystal Oscillator). It accomplishes the task of keeping the system synchronized to absolute time: in fact it adjusts the frequency of the VCTCXO to be an integer multiple of the PPS and also the relative phase, that is the VCTCXO is adjusted to have 10 million oscillations in the PPS period, with the first pulse having the rising edge coincident with the PPS pulse.

The 10 MHz square wave is used as reference clock for the STM32F767ZI, ARM-Cortex M7 microcontroller with 2 MB Flash, 512 kB of SRAM, clock frequency of 216 MHz , L1 cache, art accelerator, Digital Signal Processor (DSP) with Floating-point Unit (FPU). The microcontroller is interfaced via Serial Peripheral Interfaces (SPI) with the external analog-to-digital converter (ADC) MAX11960, which is a differential Successive Approximation Register (SAR) ADC with resolution of 20 bit, maximum sampling frequency of 1 MHz, dual simultaneous sampling, Signal to Noise Ratio (SNR) of 99dB, Total Harmonic Distortion (THD) of -123 dB, differential non linearity of $\pm 1$ LSB. The ADC has two independent SPIs with a shared clock, while the two SPIs of the microcontroller have two independent serial clock signals. Thus, in order to avoid electrical problems, one clock has been used for both the channels.

Data acquisition is performed in accordance to [3], using a sampling frequency of 12.8 kHz. Thus, the microcontroller supplies a 12.8 kHz sampling clock to the ADC, in order to have 256 samples for each rated period of the fundamental component (i.e. 50 Hz). The device has a differential $\pm 3\ V$ $(\pm\ V_{REF})$ input range. Thus, the signal conditioning stage produces a differential input signal centered around a common mode DC voltage of $\frac{V_{REF}}{2}$. The adopted conditioning stage has been presented in [9]. The two input stages for the respective transducers are followed by the optical insulation stages, that are identical for both channels and guarantee an insulation up to 2500 V and a bandwidth of 100 kHz. Also the output stages are identical for the two input signals. The conditioning ciruits reproduce signals for voltage and current channels that lay within the operating range of the ADC. Once that the signals are scaled down, accurately referred in time, sampled and converted to digital, microcontroller has to transmit the SVs. As regards the communication hardware interface, STM32F767ZI features a 10/100 Mbit/s EMAC (Ethernet Media Access Controller) peripheral that consists of a MAC 802.3 controller. It is in compliance with both Media Independent Interface (MII) and Reduced Media Independent Interface (RMII) to interface with the Physical Layer and supports ethernet frame time stamping as described in [8]. Furthermore it has a dedicated Direct Memory Access (DMA) controller that interfaces with the core and memories through the Advanced High-performance Bus (AHB) Master and Slave interfaces. The AHB Master Interface controls data transfers while the AHB Slave interface accesses Control and Status Registers (CSR) space. The Transmit First-In-Fisrt-Out (FIFO) buffers the data read from the system memory by the DMA, before the transmission by the MAC (media access control). Similarly, the Receive FIFO stores the Ethernet frames received until they are transferred to the system memory by the DMA.

## III. EMBEDDED MEASUREMENT FIRMWARE

The microcontroller has been programmed using Standard C Language. The firmware implements the opportune drivers for all the described hardware devices and performs their coordination. Starting from the disciplined 10 MHz clock, the 12.8 kHz sampling has to be produced for the ADC. Various solutions are possible to solve this problem; most of them, however, involves firmware latency. The only one that completely avoids this issue is the use of the 10 MHz clock as the main oscillator for the entire microcontroller. In this way, in fact, all the internal clocks of the microcontroller are locked in frequency and phase with the absolute time and it is possible to construct the time base for the ADC using only internal hardware devices, without involving execution time latency due to firmware routines. In particular the time base for the ADC has been built up by making use of an internal timer as key peripheral. Sum-

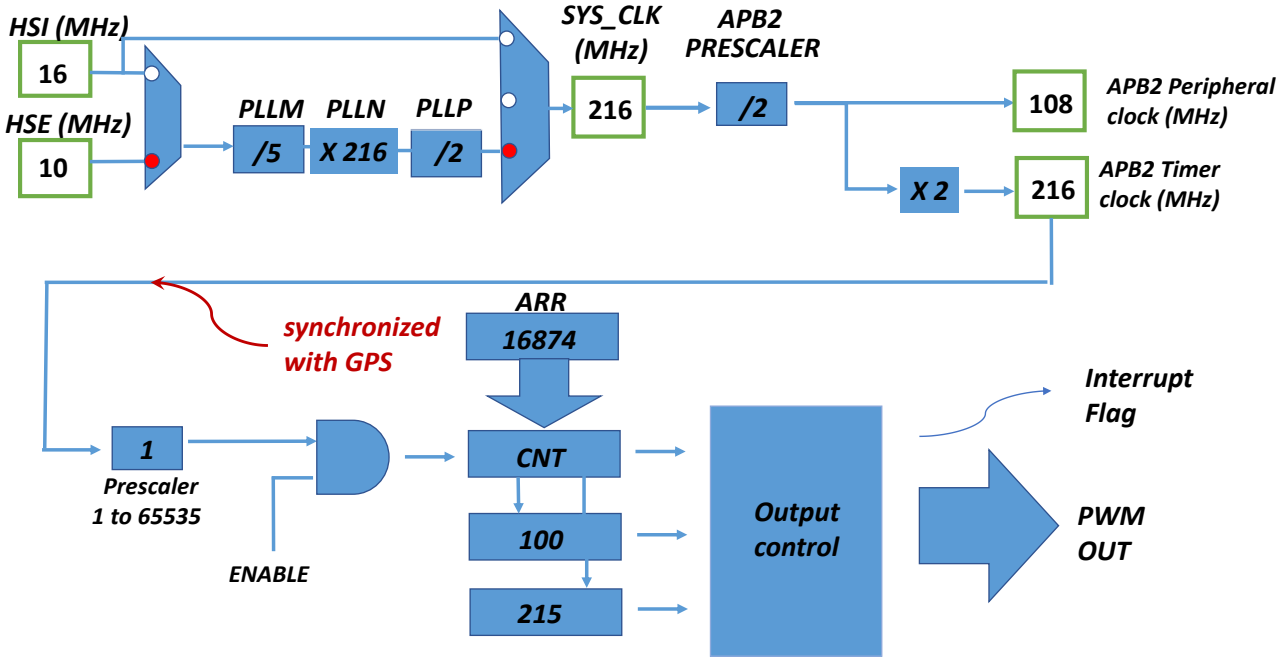


*Fig. 2. Clock configuration.*

marizing, the 10 MHz clock reference signal from GPSDO has been used as external source and given to the internal microcontroller PLL (Phase Locked Loop) circuit which allows to increase the frequency up to 216 MHz. The timer peripheral acts as divider, automatically controlling external PWM (Pulse Width Modulation) line with 50 % duty cycle. This line is used to clock the ADC. To maintain a high level of accuracy, Interrupt Service Routines (ISR) have been avoided and the timer is configured to control the output in hardware, without latency. Fig. 2 shows the block diagram of sample clock generation. System clock ($SYS\_CLK$) is obtained by the equation (1) and is equal to 216 MHz.

$$SYS\_CLK = \frac{HSE \cdot PLLM \cdot PLLN}{PLLP} \qquad (1)$$

The timer accurately divides by 16875 the system clock, to generate a 12.8 kHz square wave using the PWM output. The standard PWM mode is programmed with the Auto-Reload Register (ARR) and the Capture Compare Register (CCR) to define period and duty cycle respectively. When the counter matches the content of CRR1, the output is turned off. When counter matches ARR, the counter is set to 0, the output is turned on and the counter starts counting up again. As mentioned in section 1, the aims of the presented work is to realize a reference SAMU. According to [10], the requested accuracy for the highest time performance class (i.e. T5) must be $\pm$ 1 $\mu s$. The use of GPSDO offers significant advantages in terms of synchronization accuracy.

Moreover, the microcontroller firmware receives and parses NMEA (National Marine Electronics Association) sentences from GPS receiver to obtain timestamp. Since the SAMU must associate a timestamp to each sample, a hard real-time mechanism has been implemented to identify the precise instant in which a 1-second-frame starts, using PPS signal external interrupt. Obviously this synchronization is needed only on the first PPS frame at startup. From this moment, the system proceeds counting up each sample time and following eventual corrections carried on by GPSDO. The firmware checks this correction process monitoring the difference between internal counters (locked on disciplined 10 MHz from DSO) and NMEA time strings (locked on PPS signal from GPS system). This difference must converge in the interval $\pm$200ns within a fixed timeout.

The microcontroller is responsible for IEC61850-9-2 communication via Ethernet, too. To fulfill this task, integration between the Lightweight Internet Protocol stack (LwIP) and libiec61850[11] (an open source implementation of the standard) has been realized. This integration has been conducted through Berkley Software Distribution (BSD) socket interface in LwIP stack. IEC 61850-9-2 is based on RAW socket, not fully supported by LwIP; it has been necessary to extend that support, opportunely modifying the whole library code.

For the data-acquisition from external ADC, a producer-consumer design pattern has been chosen. The samples' reading is achieved through the event-based state machine shown in Fig. 3. The transition between the states is interrupt-based. This way, the microcontroller can perform

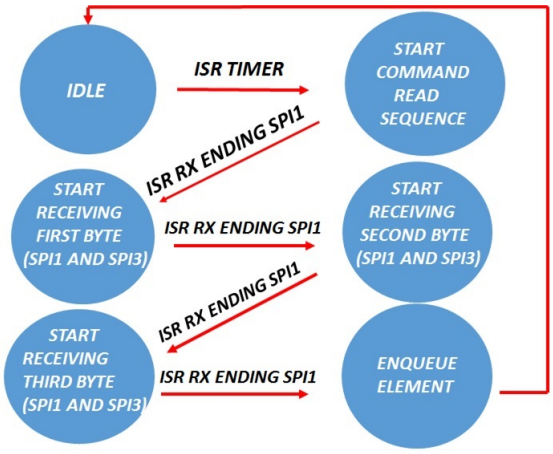


*Fig. 3. ADC samples collection via SPI.*

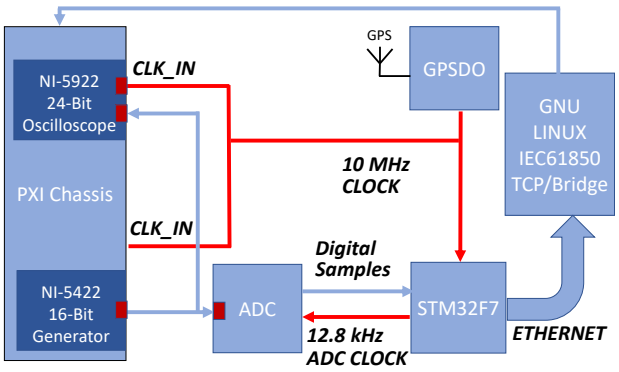


*Fig. 4. Experimental test setup.*

other tasks like sending the sample frames through the ethernet. Once the timer is enabled and started in PWM mode a 12800 Hz square wave synchronized with GPS is produced and used as conversion starter for both MAX11960 channels A and B in order to have a simultaneous sampling between voltage and current signals. The rollover timer ISR has been used to start the finite state machine; from this moment on, it evolves by interrupts from the Serial Peripheral Interface (SPI) used for data transfer from the ADC.

## IV. EXPERIMENTAL TEST

The block diagram of the measurement setup for SAMU characterization is shown in Fig. 4 [12–14]. A characterization of the system has been conducted. In particular the Effective Number Of Bit (ENOB) of the ADC and the synchronization accuracy were evaluated.

For the evaluation of the ENOB, a NI PXI (National Instruments PCI eXtension for Instrumentation) chassis, housing the NI-5422 (16 Bit, $\pm$ 12 V, 200 MHz Arbitrary Waveform Generator, AWG) and the NI-5922 (24 Bit, $\pm$ 5 V, 500 kHz Data Acquisition Board, DAQ) have been used.

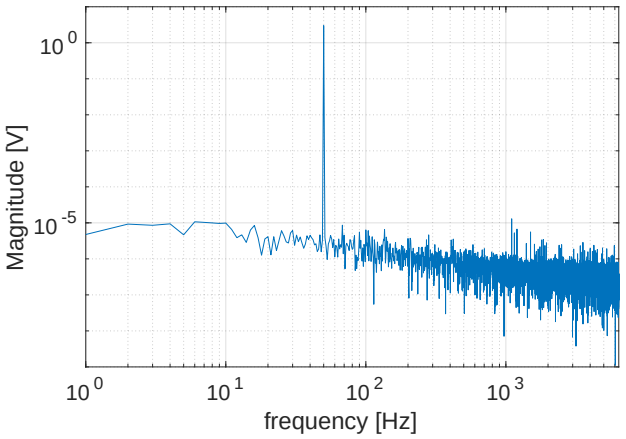


*Fig. 5. Magnitude spectrum of compensated signal.*

The PXI chassis has been supplied with a 10 MHz external clock source from the GPSDO. Both boards have been configured to use the PXI clock as reference clock in order to have coherent sampling between NI-5422, NI-5922 and proposed reference SAMU under test.

A sinusoidal signal, with amplitude equal to the ADC full scale and frequency of 50 Hz, has been used as test signal and directly supplied (excluding conditioning stages) to both the SAMU ADC and to the DAQ.

Using the DAQ as reference device, a closed loop compensation has been implemented, to enhance the test signal spectral purity. The sine wave obtained with this technique reaches a SINAD (Signal to Noise And Distortion Ratio) over 92 $dB$; its magnitude spectrum, obtained without the parallel connection of the SAMU ADC, is reported in Fig. 5). Unfortunately, when parallel connecting the SAMU ADC, the closed loop compensation does not give the same performance. In fact, as depicted in Fig. 6, which shows the magnitude spectrum of the signal present at the ADC input measured during the test, the spectral purity becomes lower as the SINAD drops to about $85dB$. Obviously, such spectral purity is not enough to characterize the rated ADC amplitude resolution of 20 bits. Further studies are still in progress to solve load effect issue and to enhance the spectral purity of the test signal.

The software for the measuring setup has been developed in LabVIEW under Windows OS (Operating System). Unfortunately, Windows reveals to have poor support for RAW socket. For this reason, the measurement results, i.e. the sampled values of the SAMU, are sent via ethernet to a IEC 61850-9-2/TCP (Transmission Control Protocol) bridge (realized using [11]) and subsequently to the PXI controller.

In Fig. 7 the magnitude spectrum of the sampled values is reported. The presence of the same harmonics of the input test signal can be seen. Moreover it is important to

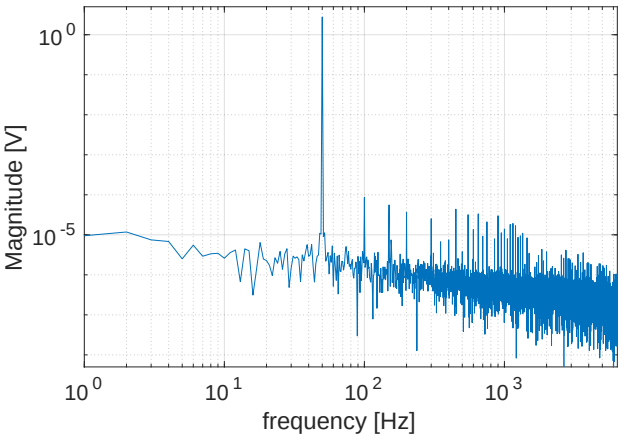


*Fig. 6. Magnitude spectrum of test signal with load effect.*

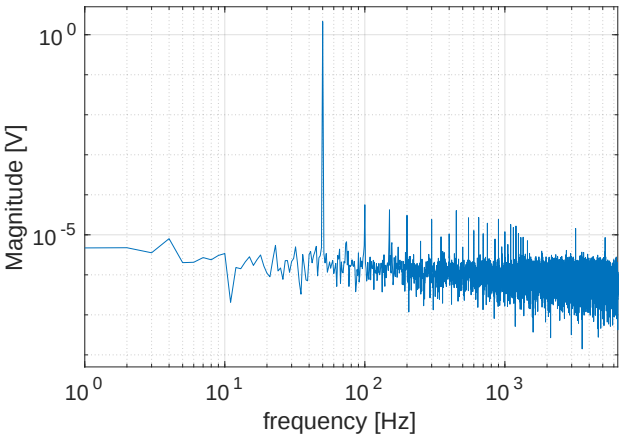


*Fig. 7. Magnitude spectrum of ADC samples.*

highlight that there is an undesired spectral component at exactly 3200 Hz, not present in the input signal. For this reason the SINAD at the ADC output never exceeds 84 dB.

This spurious spectral component is uncorrelated with the input signal; to prove that consideration, another test has been conducted putting zero volt at the input of the ADC (with a short circuit). As it can be seen from Fig. 8, the undesired tone is still present, located at the frequency $f_d = 3.2\ kHz$. Investigations about this issue (changing the sampling frequency and/or changing the clock signal amplitude and frequency), led to realize that the disturbance is due to capacitive coupling with the 10 MHz clock signal. This last frequency is aliased according to equation (2).

$$f_d = |f_{clock} \pm k \cdot f_s| \tag{2}$$

where $f_{clock}$ is the clock signal at 10 MHz and $f_s$ is the the sampling frequency of 12.8 kHz; choosing $k = 781$ the $f_d$ results exactly equal to 3.2 kHz.

Despite its small amplitude, the spurious component is considerably higher than the noise floor. Further efforts, to enhance the performance of anti-aliasing filter at the input of ADC, are in progress.

In order to evaluate the time synchronization accuracy of the proposed SAMU, other experimental tests have been conducted. An Agilent 53230A Universal Frequency Counter has been used to determine the conversion starter stability. The experimental results show that a standard deviation of 10 $\mu$Hz on the sampling frequency has been obtained. Furthermore the maximum error on sampling period, measured on 10 minute observation time, is about 200 ns [10]. Further experimental tests to evaluate the synchronization error with respect to the absolute time are still in progress.

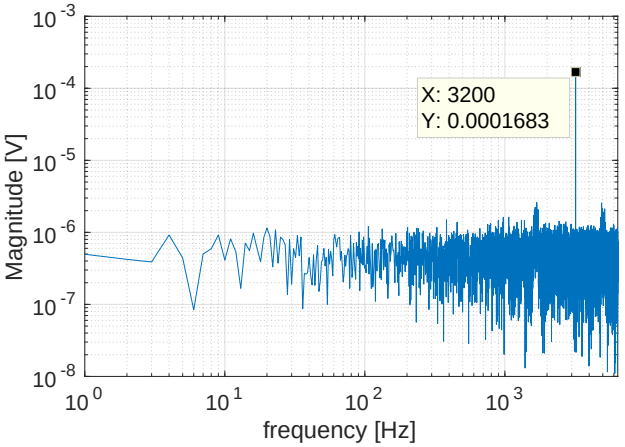


*Fig. 8. Magnitude spectrum of ADC samples with a short circuit at the input.*

## V. CONCLUSION

This paper discusses the implementation of a reference Stand Alone Merging Unit, based on an ARM microcontroller. It also includes an external high resolution ADC, a conditioning stage, to adapt voltage and current signals coming from VTs and CTs to ADC input range, and a GPSDO. Experimental results to evaulate the ENOB and the stability of the timebase have been presented.

Further experimental tests of the realized SAMU are still in progress, in order to obtain a complete metrological characterization of the proposed reference instrument. Moreover, various solutions are being evaluated to reduce or possibly eliminate spurious spectral component due to capacitive coupling.

## VI. ACKNOWLEDGEMENT

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REFERENCES

[1] **G. Crotti**, **D. Giordano**, **A. Delle Ferninc**, **D. Gallo**, **C. Landi**, and **M. Luiso**. A testbed for static and dynamic characterization of dc voltage and current transducers. *9th IEEE International Workshop on Applied Measurements for Power Systems, AMPS 2018 - Proceedings*, 2018.

[2] **G. Crotti**, **D. Giordano**, **P. Roccato**, **A. Delle Femine**, **D. Gallo**, **C. Landi**, **M. Luiso**, and **A. Mariscotti**. Pantograph-to-ohl arc: Conducted effects in dc railway supply system. *9th IEEE International Workshop on Applied Measurements for Power Systems, AMPS 2018 - Proceedings*, 2018.

[3] Communication networks and systems for power utility automation - part 9-2: Specific communication service mapping (scsm) - sampled values over iso/iec 8802-3. *IEC EN 61850-9-2:2011*, Sep 2011.

[4] **M. Agustoni** and **A. Mortara**. A calibration setup for iec 61850-9-2 devices. *IEEE Transactions on Instrumentation and Measurement*, 66(6):1124–1130, June 2017.

[5] **A. Delle Femine**, **D. Gallo**, **D. Giordano**, **C. Landi**, **M. Luiso**, and **D. Signorino**. Synchronized measurement system for railway application. *Journal of Physics: Conference Series*, 1065(5), 2018.

[6] **G. Crotti**, **A. Delle Femine**, **D. Gallo**, **D. Giordano**, **C. Landi**, and **M. Luiso**. Measurement of the absolute phase error of digitizers. *IEEE Transactions on Instrumentation and Measurement*, 68(6):1724–1731, 2019.

[7] Communication networks and systems for power utility automation - part 9-3: Precision time protocol profile for power utility automation. *IEC EN 61850-9-3:2016*, May 2016.

[8] Ieee standard profile for use of ieee 1588 precision time protocol in power system applications. *IEEE Std C37.238-2017 (Revision of IEEE Std C37.238-2011)*, pages 1–42, June 2017.

[9] **S. Del Prete**, **A. Delle Femine**, **D. Gallo**, **C. Landi**, and **M. Luiso**. Implementation of a distributed stand alone merging unit. *Journal of Physics: Conference Series*, 1065:052042, aug 2018.

[10] Communication networks and systems in substations - part 5: Communication requirements for functions and devices models. *IEC EN 61850-5:2004*, Nov 2014.

[11] Official repository for libiec61850, the open-source library for the iec 61850 protocols, availabble online on 01.06.2018 at http://libiec61850.com/libiec61850.

[12] **A. J. Collin**, **A. Delle Femine**, **D. Gallo**, **R. Langella**, and **M. Luiso**. Compensation of current transformers' non-linearities by means of frequency coupling matrices. In *2018 IEEE 9th International Workshop on Applied Measurements for Power Systems (AMPS)*, pages 1–6, Sep. 2018.

[13] **A. Cataliotti**, **V. Cosentino**, **G. Crotti**, **A. Delle Femine**, **D. Di Cara**, **D. Gallo**, **D. Giordano**, **C. Landi**, **M. Luiso**, **M. Modarres**, and **G. Tine'**. Compensation of nonlinearity of voltage and current instrument transformers. *IEEE Transactions on Instrumentation and Measurement*, 68(5):1322–1332, May 2019.

[14] **G. Crotti**, **A. Delle Femine**, **D. Gallo**, **D. Giordano**, **C. Landi**, **P.S. Letizia**, and **M. Luiso**. Calibration of current transformers in distorted conditions. *Journal of Physics: Conference Series*, 1065:052033, aug 2018.