Low-cost Implementation of an Active Phasor Data Concentrator for Smart Grid

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*Abstract*— Nowadays, synchrophasor technology is becoming an important element for monitoring power systems. The base elements of the measurement architecture are represented by the Phasor Measurement Unit (PMU) and the Phasor Data Concentrator (PDC). The PMU is the “sensor” of the measurement system and the PDC is the collector of the data forwarded by PMUs installed on the field. Recently, several research works and pilot projects are pushing to extend the benefit of synchrophasor technology from transmission grids to distribution networks. In this context, different projects are seeking to use low-cost platforms to design devices with PMU functionalities. In this perspective, to achieve a complete measurement architecture based on low-cost synchrophasor technologies, this work presents a PDC design based on a low-cost platform, in which, despite the simplicity of the considered hardware, advanced PDC functionalities are implemented. The proposed device is evaluated through the performance of the time synchronisation module and the number of data streams, compliant with standard IEEE C37.118.2-2011, that can be managed at different reporting rates.

Keywords— Phasor Data Concentrator (PDC); IEEE C37.118.2; Synchrophasor Technology; Single Board Computer; Raspberry Pi, Smart Grid.

# Introduction

The measurement devices used in the power networks monitoring systems based on synchrophasor technology comprise Phasor Measurement Units (PMUs) and Phasor Data Concentrators (PDCs) [1]-[3]. The PMU is the “sensor” of the measurement system and gives several measurements: synchronized phasor magnitude and phase angle, frequency and Rate of Change of Frequency (ROCOF), evaluated from voltage and current signals [4]. All the measurements are time-tagged using an absolute time reference in Universal Coordinated Time (UTC) format and usually provided by the Global Positioning System (GPS). Measurements are encapsulated in data packets compliant with the standard IEEE C37.118.2 [5] and forwarded to the PDC. The data coming from PMUs in the field are thus collected by the PDC and typically forwarded in suitable streams to the control centre. In the control centre, different applications are implemented to use PMU data for the target applications. Data can be used for real-time analysis but also stored for off-line analysis.

Synchrophasor technology was originally designed to monitor transmission systems. Nowadays, research is pushing to extend the benefits of synchronised measurements to distribution networks. Due to different scale and economic constraints with respect to transmission systems, ongoing industrial and academic research projects are working to exploit low-cost architectures for PMU implementation [6]-[9].

A PMU project based on low-cost hardware can be developed using the most common Single Board Computer (SBC) platforms. Thanks to the low cost, the good performance and the availability of varied hardware equipment that can be integrated into the boards (as wireless and wired communication), these devices are pushing the development of prototypes specifically designed for the IoT architecture [10].

The PDC is designed to collect and align measurements with the same timestamp and to forward the data to upper levels of the architecture. It is thus the first element of the synchrophasor system with a global view of an entire portion of the electric system, thanks to measurement data received from different locations in the field [11]. In this context, the PDC could be engineered as a new measurement device able to make decisions relying on the information received from different sources.

Currently, commercial PDCs suitable for transmission system monitoring allow managing hundreds of incoming streams (in IEEE C37.118.2 format [5]). The cost of a PDC is in the order of thousands of dollars. These devices can implement mathematical functions (power calculations, evaluation of sequence components) and other utility functions, such as alarms, that are specific for electric substations; however, this equipment is not usually programmable by users for specific functions.

This paper presents an active low-cost PDC suitable for distribution networks. The main objective is to allow the implementation of advanced functionalities, and, in particular, time-related measurements, which enable advanced stream management [11]. The prototype is based on the most common SBC, the Raspberry Pi [12]. The characterisation of the device is twofold, aimed at the evaluation of both the time accuracy provided by the Global Navigation Satellite System (GNSS) receiver connected to the board and the supported load, which is expressed in terms of the number of data streams that the system is able to manage without a decline in performance.

# The Proposed Architecture

The proposed architecture is based on two low-cost hardware devices and on a software application developed in LabVIEW environment. The cost of the overall hardware is less than € 80. Fig. 1 describes the prototype and the development environment.



1. Proposed PDC prototype based on SBC Raspberry Pi 3B and Uputronics synchronisation board.
	1. *Hardware*

The PDC prototype is developed using the low-cost SBC Raspberry Pi, produced by the Raspberry Pi Foundation [12]. The SBC is the model 3B equipped with a System on Chip (SOC) BCM2837 with a CPU quad-core ARM up to 1.2 GHz and 1 GB of RAM. The SBC is also equipped with a 10/100 ethernet and a 2.4 GHz Wi-Fi 802.11n modules, which make the device able to receive the streams provided by the PMUs. A 40 pins GPIO (General Purpose Input/Output) is used to communicate with the peripherals and to generate the digital signal shown in the next section. The device does not comprise a real-time clock, but, for the implementation of the active functionalities defined in [11], an accurate time reference is necessary to evaluate correctly the latency of the data packets received from each connected PMU. To overcome this lack, the prototype is equipped with a Uputronics GPS expansion board including a GNSS receiver. The U-Blox MAX-M8Q module is able to provide the absolute time reference pulse per second signal (PPS) with an accuracy of ± 60 ns.

* 1. *Software*

The operating system used in the SBC is the Linux Raspbian, based on Debian. The software of the proposed active PDC is developed under LabVIEW environment. Communication between the development PC and the LabVIEW project in the prototype is managed by the hardware abstraction layer provided by the LINX firmware installed in the SBC. The virtual instrument (VI) running in the SBC exploits the LINX firmware that provides the necessary logic to access the SBC and GPIO interfaces [13].

# Test Setup and Results

To validate the feasibility of the proposed approach, the performance of the prototype is characterized through a suitable test setup and three different test sections. The first one concerns the capability to evaluate the latency of the incoming data streams and the associated accuracy level. The second testing stage is focused on the performance of the prototype while dealing with multiple incoming data streams. In this case, the CPU utilisation level of the SBC is used as an index of performance. In the last test set, the PDC prototype is included in a real synchrophasor architecture, based on two commercial PMUs, compliant with the last version of synchrophasor standard IEEE C37.118.1a [2], and one PDC, with the aim to evaluate the overall latency of the synchrophasor monitoring system while varying the architecture and considering the latency contributions for each component.

* 1. *Time Synchronisation*

A good level of time synchronisation is a prerequisite to evaluate the latency of every incoming stream. The proposed PDC, provided with latency evaluation functionality, reads the time-tag included in every data packet (in the SOC and FRACSEC fields of the IEEE C37.118.2 data frame header) of incoming PMU streams and evaluates the delay between it and the arrival time of the data packet. This approach requires an arrival time measurement with a sufficient accuracy and thus a source of synchronization for the PDC timebase [11].

Fig. 2 shows the test setup to evaluate the accuracy of the time synchronisation of the prototype.



1. Experimental setup designed to evaluate synchronisation performance of the PDC prototype.

The test setup is composed of a GPS receiver Symmetricom XL-750 able to generate the synchronisation time signal (PPS) up to 50 Hz with an accuracy of ±100 ns. The PDC prototype is programmed to generate a digital signal every second using the GPIO of the SBC as shown in Fig. 1. This digital signal is generated to keep the pace of the occurrence of the UTC second in the LabVIEW environment.



1. Time offset between the PDC prototype and GPS receiver.

 The two synchronisation signals (from GPS and from prototype) are acquired and the time offset is evaluated using counter functionality of the National Instruments DAQ board USB-6211, connected to a PC desktop via USB.

Fig. 3 shows the time offset measured over five hours, that is considering the 18000 measurements corresponding to second occurrences. The distribution of the time offset is shown in Fig. 4: the mean value is 164.4 µs and the standard deviation 14.1 µs. The maximum offset obtained in the test is 297.4 µs and the jitter, defined as the difference between maximum and minimum time offset, is 170.7 µs.

In this test, the time offset is directly obtained by PPS signals comparison and no correction has been added. Nevertheless, it is clear from the results that a compensation of the average time offset would be effective in reducing the synchronization error. This can be done by adjusting the generation trigger in the LabVIEW application. Anyway, the synchronisation level obtained by the prototype is fully adequate to evaluate the latency of a PMU data stream as reported in [2], where a 2-ms time accuracy is required.

* 1. *CPU utilisation*

Fig. 5 represents the test setup to evaluate the performance of the PDC prototype in terms of CPU utilisation with 10 incoming data streams. The data of the different streams are individually collected and evaluated in terms of latency. During this test, no other operations are selected in the PDC prototype. The PMUs simulator, which relies on a PMU data stream simulator software developed in LabVIEW, can generate data streams compliant with the standard IEEE C37.118.2 with different reporting rates. The TCP communication is used between the PMUs simulator and PDC prototype. PMUs simulator runs in a PC desktop synchronised by the local area Network Time Protocol (NTP) every 15 minutes, and its clock is also used to countercheck for anomalous behaviour during tests.



1. Histogram of the time offset between the PPS generated by the PDC prototype and that of the GPS receiver (5 h measurements).



1. Experimental setup designed to evaluate the CPU utilisation of the PDC prototype with 10 streams from simulated PMUs.
2. Values of CPU utilisation with 10 incoming streams of PMU data and Different Reporting Rates

|  |  |
| --- | --- |
| Reporting Rate (Fs)[fps] | CPU Utilisation [%] |
| 1 | 6 |
| 10 | 9 |
| 25 | 15 |
| 50 | 23 |

Table I reports the results in terms of CPU utilisation with 10 streams when different reporting rates up to 50 fps are considered. It is clear that the prototype can manage without problems 10 streams up to the maximum reporting rate prescribed by the standard IEEE C37.118.1 [1], which is 50 fps for a system operating at the nominal frequency of 50 Hz.

* 1. *Real Architecture Scenario*

In the first part of the tests, focusing on a real architecture scenario, the PDC prototype is configured to collect and evaluate the PMU latency for two incoming streams of measurement data provided by two commercial PMUs (Fig. 6).

Each element of this architecture is synchronized with the UTC and the PDC prototype can evaluate the synchrophasor data latency including both PMU and network latencies.



1. Experimental setup designed to evaluate synchrophasor data latency with the PDC prototype.

The limits of PMU latency (the so-called PMU reporting latency) given in [2] are reported in Table II. The latency value is associated with the measurement process of the devices and strictly depends on two main PMU characteristics: the performance class and the reporting rate.

1. Maximum PMUs reporting latency in [2]

|  |  |
| --- | --- |
| Performance Class | Maximum PMU reporting Latency [s] |
| P  | 2/Fs |
| M | 7/Fs |

The PMUs are connected to the PDC through a 10/100 commercial Ethernet switch in a laboratory test setup without other types of network traffic.

1. Evaluation of the synchrophasor data latency (Fs = 10 fps)

|  |  |  |  |
| --- | --- | --- | --- |
| PMU | Max[ms] | Mean [ms] | St. Dev.[ms] |
| PMU A | P | 66.7 | 66.2 | 0.2 |
| M | 583.4 | 582.7 | 0.2 |
| PMU B | P | 73.8 | 73.2 | 0.1 |
| M | 718.2 | 713.4 | 0.2 |

1. Evaluation of the synchrophasor data latency (Fs = 50 fps)

|  |  |  |  |
| --- | --- | --- | --- |
| PMU | Max[ms] | Mean[ms] | St. Dev.[ms] |
| PMU A | P | 71.0 | 70.5 | 0.1 |
| M | 134.9 | 134.8 | 0.1 |
| PMU B | P | 73.4 | 73.0 | 0.1 |
| M | 168.0 | 167.0 | 0.1 |

The results of the synchrophasor data latency evaluation over 1000 TCP messages are shown in Tables III and IV for reporting rates of 10 fps and 50 fps, respectively.

The tables report the results for both performance classes in terms of maximum and mean values and standard deviations. The chosen $F\_{s}$ values are the minimum and maximum mandatory reporting rates prescribed in [1].

It is worth recalling that, the P class is specific for applications that require low latency and its measurement error requirements do not significantly change for the used reporting rates. For this reason, in the implementation, the same algorithm is adopted by manufacturers and this leads to two very similar latency results as indicated by the results.

On the contrary, requirements for the M-class are different for each reporting rate and, as shown in the Tables III and IV, the values of latency largely increase with lower reporting rates.

The second test case is based on a synchrophasor architecture comprising two PMUs and an intermediate PDC layer (Fig. 7).



1. Experimental setup designed to evaluate PDC reporting latency of the WAMS system.

The commercial PMUs send their outputs to a workstation (equipped with an I7 quad-core Intel processor, 8 GB ram, and Windows 7 operating system) provided with OpenPDC software [14]. OpenPDC implements the PDC functionality to collect, align, and forward, in a single output stream, the received input data to the low-cost PDC, following the hierarchical architecture suggested in [1].

The workstation is equipped with two Ethernet interfaces: the first one is connected to a switch to receive the incoming PMU streams and the second one is directly connected through an Ethernet cable to the PDC prototype. Since PMUs are connected to the unsynchronized OpenPDC system, the PDC prototype is in charge to evaluate the overall latency of the input stream, which practically corresponds to the intermediate PDC output latency. Comparing these new results with those of the previous test case, it is possible to evaluate the latency generated by the intermediate PDC.

1. Evaluation of the latency with an Intermediate PDC

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Fs[fps] | Input streamstype | Max[ms] | Mean[ms] | St. Dev.[ms] |
| 10 | P | 1015.4 | 1012.6 | 0.4 |
| M | 1001.3 | 998.8 | 0.4 |
| 50 | P | 1013.8 | 1009.5 | 0.4 |
| M | 1024.2 | 999.7 | 0.4 |

Table V reports the latency measurements over 1000 TCP messages when either P or M class is considered for both PMUs and with reporting rates of 10 fps and 50 fps.

The results in terms of maximum latency are similar for the two performance classes. This may be attributed to the OpenPDC software, whose default configuration includes a one-second waiting time (lag time) before transmitting the aligned data. Any data arriving after that interval has elapsed are considered as late and are discarded. It is clear from the results that PDC configurations can play a crucial role in the overall system performance. The above OpenPDC configuration is useful to send data within a fixed time frame, but it strongly affects the propagation through the system layers. If measurements are used for fast response applications, then this configuration may make useless the benefits of the P-class PMUs in terms of speed. The proposed synchronized PDC proves to be a valuable tool to evaluate in real-time the operating conditions of even complex architectures.

# Conclusion

Synchrophasor technology is becoming an important tool for operators to monitor in real-time the electric systems over a wide area. Currently, this technology is viewed with interest not only for transmission grids but also for distribution networks. In this context, with the aim of exploring the possibilities for synchrophasor-based monitoring architectures, this paper has presented a prototype of an active PDC developed with low-cost hardware. The feasibility of the proposal was evaluated through the capability of the system to deal with time synchronisation at a good level of accuracy, thus enabling also nontrivial data managing. The prototype is also able to safely manage several PMU data streams with different reporting rates and is thus promising as a building block for complex smart grid monitoring architectures. The evaluation of synchrophasor data latency in these hierarchical architectures is also important for a real-time monitoring of the latency conditions at different levels. The proposed PDC can be helpful also to reveal improper configurations of a lower-level PDC software or malfunctions in the synchrophasor data routing.

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