21st IMEKO TC4 International Symposium and
19th International Workshop on ADC Modelling and Testing
Understanding the World through Electrical and Electronic Measurement
Budapest, Hungary, September 7-9, 2016

Skeleton last edited: 02-Aug-2015 18:34

Extended Abstract Submitted for Review

Symposium topic(s): Sensor and Transducers

Experimental Characterization of Bandwidth Limits in Hall Sensors

M. Crescentini[1], P. A. Traverso[1], P. Alberti[2], A. Romani[1,2], M. Marchesi[3], D. Cristaudo[4], R. Canegallo[3], and M. Tartagni[1,2]

[1]*DEI, University of Bologna, 47521 Cesena, Italy, marco.crescentini3@unibo.it*
[2]*ARCES, University of Bologna, 47521 Cesena, Italy*
[3]*Analog & Smart Power Technology, STMicroelectronics, 20010 Castelletto (MI), Italy*
[4]*Analog and MEMS Group, STMicroelectronics, 95121 Catania (CT), Italy*

Abstract – **Modern power applications are demanding for broadband current sensors. Hall sensors are a good solution from a general standpoint, but practical implementations are limited to a few hundred kHz. In fact, many parasitic dynamic effects perturb the time response of the Hall sensor, making difficult to experimentally assess the fundamental frequency limit and achieve it in the applications. This paper presents an equivalent electrical model that helps to design a test aimed at experimentally estimating the intrinsic time response of the sensor. According this test, the paper demonstrates that Hall sensors have an upper bandwidth limit defined by the overall capacitive load. Moreover, some of the parasitic dynamic effects, which degrade the time response in real operation, are identified and investigated.**

Keywords – **Hall sensor, Current sensor, Silicon Hall element, Wide bandwidth, Hall sensor model.**

I. INTRODUCTION

Current sensors are key elements in the design of many power systems, such as motor drivers or power converters [1]. Modern power applications, like power management in electric vehicles, are demanding for current sensors with state-of-the-art performance in terms of bandwidth, linearity, isolation, power consumption, and many other requirements [1-3]. Among these specifications, wide bandwidth (i.e., from DC to several MHz) is the most challenging [1,3]. Nowadays, wide bandwidth current sensors are commonly implemented by means of resistive shunts or current transformers (CT). The formers are relatively cost-effective but are quite bulky and realise non-isolated measurement; the latters do realise isolated measurement but they are bulky, quite expensive and suffer from magnetic saturation.

Current sensing based on the Hall effect is very promising in terms of size, cost and power consumption, since the Hall sensing element can be easily integrated in a CMOS System-on-Chip (SoC). However, practical realizations still have limited bandwidth. Commercial silicon-based Hall sensors are commonly limited to the 10 – 100 kHz bandwidths [4,5]. The fastest Hall sensor available in the market is the Asahi Kasei CQ3300, with a bandwidth of 1 MHz [6], but it is implemented using non-standard semiconductor compounds.

The physics-based description of Hall elements suggests three main bandwidth-limiting high-frequency effects: i) relaxation time of the carriers; ii) inductive effects; iii) capacitive effects [7]. A recent paper by the authors demonstrated, by means of numerical simulations, that capacitive effects define the fundamental frequency upper limit [8]. This paper presents an equivalent electrical model describing the dynamic response of the Hall sensing element. Based on this model, the paper identifies a test able to experimentally demonstrate that capacitive effects actually determine the fundamental frequency limit. However, several parasitic dynamic effects superimpose and further perturb the actual time response of the Hall element, degrading it with respect to the intrinsic capacitive-limited time response. Some of those parasitic effects are identified and investigated.

II. HALL SENSOR

A. Theory and Electrical Model

When a current I_b flows through a ribbon of material and a magnetic field B is applied orthogonally to the ribbon surface, the charge carriers in the material bend from their original path and a small voltage V_H arises orthogonally to both I_b and B. This Hall voltage V_H is given by the formula:

$$V_H = S_I \cdot I_b \cdot B \tag{1}$$

where S_I is the current-related sensitivity of the Hall element and depends on geometrical and physical properties [1]. The Hall sensing element is commonly realized by means of semiconductors, rather than metals, due to their lower charge carrier mobility. In the following, we will refer to a square silicon Hall element realized by a thick n-well, which constitutes the sensing area, surrounded by a lowly doped p-substrate and connected to the embedding electronic circuits by four square contacts realized by means of highly doped n^+ implantations (Fig. 1) The Hall sensor is provided by STMicroelectronics and it is realized in BCD 0.16 µm technology.

The Hall element is intrinsically a magnetic sensor, as defined in eq. (1). To convert it into a current sensor, a copper strip is deposited 2 µm above and 70 µm far the sensing element, as shown in Fig. 2-a and Fig. 2-b. Assuming a pure algebraic relation between B and current I, which flows through the copper strip, then V_H is given by:

$$V_H = S_I \cdot I_b \cdot \frac{\mu_s}{2\pi r} \cdot I \tag{2}$$

where r is the radial distance between the Hall element and the copper strip and μ_S is the silicon permeability (that is almost equal to the vacuum permeability).

Summarizing, the current I (i.e., the measurand) generates a magnetic field B that impresses on the Hall element and deflects charge carriers from their original path, hence it creates a local transversal charge re-distribution and a related voltage drop V_H. Based on the above description, we propose the two-port, parallel RC-based model of Fig. 2-c. This model is in agreement with the basic theory of Hall effect [7], given

$$R_{eq} = G_H \cdot R_{sq} \tag{3}$$

$$I_H = K \cdot I = \frac{L}{W} \mu_H I_b \frac{\mu_s}{2\pi r} \cdot I \tag{4}$$

where G_H is a geometrical factor, R_{sq} is the well square resistance, L and W are well sizes and μ_H is the Hall mobility. The current I_H can be treated as the Hall current, that represents the transversal local movement of carriers due to the Lorentz force. The voltage generator V_{off} placed in series to the resistance R_{eq} models the offset voltage due to technology and process. The black-box that embeds the parallel RC is aimed at taking into account all the parasitic physical phenomena that are not described by the intrinsic core of the model, such as induced electromotive force (emf), magneto-resistivity, additional inductive effects, electrical coupling among the pins of the Hall element and so on.
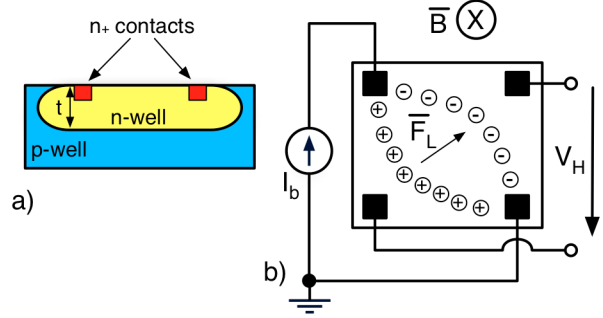

Fig. 1 a) Lateral section of the Hall sensor and b) scheme showing the Hall effect and the connections of the Hall sensor with surround circuits.
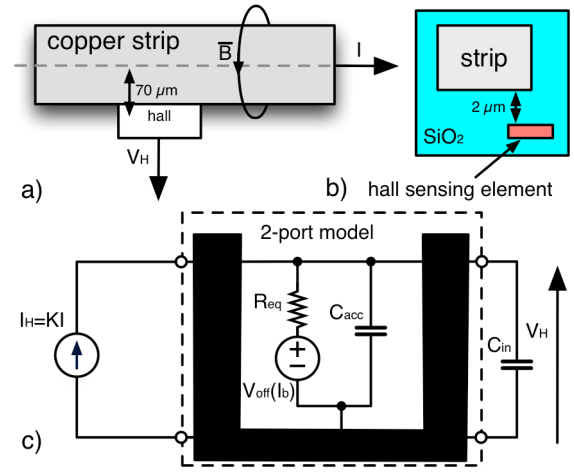

Fig. 2 a) The sensed current I flows through a copper strip placed 2 µm above and 70 µm far from the Hall sensing element. b) cross section highlighting the vertical displacement between metal strip and Hall element. c) 2-port model of the Hall-based current sensor.

B. Bias Current Spinning Technique

Hall elements suffer from a significant offset voltage V_{off}. This offset is due to charge accumulation that is present even in absence of a magnetic field. The common technique to minimize the effect of this high offset voltage is the spinning technique [1,3,4]. It involves a periodical 90 degrees rotation of the bias current and the averaging over the four corresponding measurements [5]. The technique is very effective but adds another limit in the speed of the sensor, since the carriers must correctly rearrange in space accordingly to the new bias direction. The offset voltage is a function of I_b [6]. Hence, accordingly to the model of Fig. 2-c, the time variations of I_b trigger the same RC time constant (the same charge re-distribution mechanism, from a physical standpoint) triggered by the variations of the magnetic field (i.e., of the current I), without exciting most of the other (parasitic) dynamic effects. This particular operative condition will be exploited to experimentally characterize the intrinsic RC time constant of the Hall element.

III. NUMERICAL BANDWITH LIMIT INVESTIGATION

The sensor prototype has been modelled and simulated using the physical simulator Synopsys Sentaurus Device®[1]. This tool takes into account all the typical phenomena occurring in a semiconductor device, from carrier transport model to electron-hole recombination, carrier scattering and mobility degradation. Moreover, the tool embeds an enhanced formulation of the current density that models the Lorentz force applied by a magnetic field B to the carriers flowing into semiconductor:

$$\vec{J_n} = \mu_n \vec{g_n} + \frac{\mu_n}{1+\left(\mu_H B\right)^2}\left[\mu_n^* \vec{B} \times \vec{g_n} + \mu_H \vec{B} \times \left(\mu_H \vec{B} \times \vec{g_n}\right)\right] \quad (5)$$

where $\vec{g_n}$ is the current vector with de-embedded mobility, μ_H is the Hall mobility, μ_n is the electron mobility, $\vec{B}$ is the magnetic induction vector and B is the magnitude of this vector [9]. A full description of the simulation environment, together with validation of the approach by means of static analysis, is given in [8].

The time response of the modelled Hall sensor to an instantaneous magnetic step of 40 mT with different capacitive loads is shown in Fig. 3. The sensor response is quasi-static when no capacitors are coupled to the sensor, while it shows a time constant τ of about 18 ns when it is loaded with 6 pF. The figure reports the simulation points fitted in Matlab® with spline functions. This simulation result, where main parasitic effects have
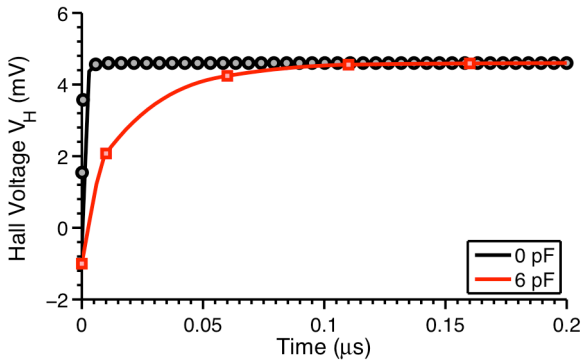
Fig. 3 Simulated time response of the square Hall sensing element to a magnetic step of 40 mT with different loading capacitances connected to the readout contacts. The sensor is DC biased with 500 μA. The resulting time constant is in good agreement with layout-extracted parameters $R_{eq}= 3kΩ$, $C_{acc}= 0.9pF$

[1] The software described in this document is furnished under a license from Synospys International Limited.

been neglected, suggests that the intrinsic, maximum bandwidth of the Hall sensing element is defined by an RC-like time constant[8]. This time constant is given by the product of $R=R_{eq}$ and the total capacitance $C = C_{acc} + C_{in}$ facing to the output nodes, where C_{acc} models the transversal, Hall effect-induced charge accumulation, while C_{in} is the capacitive load connected to readout contacts (the equation for C is rigorously true under the assumption that C_{acc} is directly connected to the output port). Note that in a realistic architecture C_{in} is the differential input capacitance of amplifier stage(s) plus capacitive parasitics. The time constant extracted from the above described simulation is in agreement with the layout-extracted parameters $R_{eq}=$ 3 kΩ and $C_{acc}=$ 0.9 pF.

IV. EXPERIMENTAL BANDWIDTH LIMIT INVESTIGATION

In the following, two batches of CMOS Hall sensors will be experimentally analysed. The Hall sensing element is the same in both batches, but they integrate different circuits. More precisely, batch a is an hybrid solution, which integrates only the Hall element, with bias and signal conditioning implemented by off-the-shelf components (Fig. 4-a); while batch b monolithically integrates the Hall element together with all the auxiliary circuits i.e., bias network and voltage amplifiers (Fig. 4-b). Given the implementation described above, case a has obviously much bigger load capacitance C_{in}, in the order of several tens of pF, and it is expected to experimentally exhibit a slower time constant, while case b is a solution that minimizes the value of C_{in}. The technological parameter C_{acc} is the same for both sensors.

The generation of fast changing magnetic fields is a difficult task. In addition, fast variations of B would excite parasitic phenomena described by the black-box in Fig. 2-c, perturbing the fundamental response of the intrinsic parallel RC. For this reason, we will measure the output voltage time response to a step of the *bias* current I_b, as discussed in Section II. This time response is measured as follows: a current I_b square-wave with zero mean is applied to the sensor through contacts A and B while no current I is injected into the sensing strip. In this way the output voltage v_{OUT} is an amplified version of the response of the intrinsic RC network in Fig. 2-c, allowing us to estimate the inherent time constant of the sensor. Bandwidth limitations of the amplifiers have been taken into consideration during result analysis.

A NI-PXI 5124 data acquisition board operated at 200 MSa/s with AC input coupling acquires the output voltages.

A. Hall Sensing Element with External Circuits

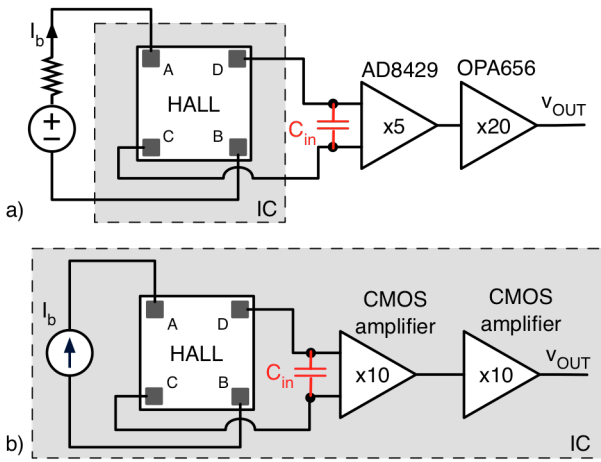The result of the test applied to the Hall element with

Fig. 4 case a): the auxiliary circuits are external to the CMOS chip integrating the Hall sensing element; case b): both Hall element and auxiliary circuits are monolithically integrated into the same substrate.
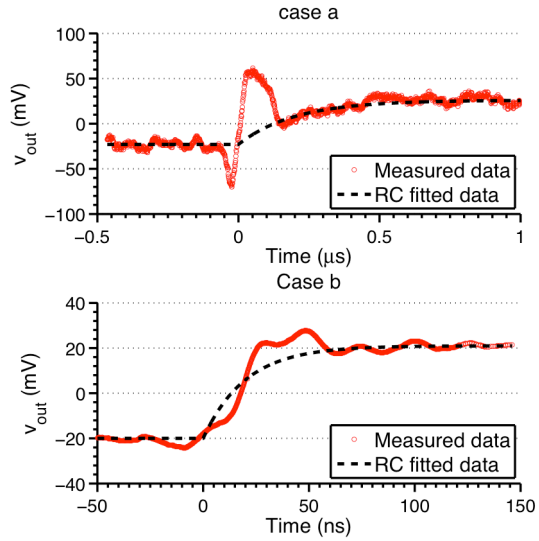
Fig. 5 Measured response to a step change of I_b, giving insights into the intrinsic RC time response for both batches of sensors Parameters extracted from the measurements are: Case a) R=3 kΩ, C=66 pF; Case b) R=3 kΩ, C=4 pF.

external auxiliary circuits (case *a*) is reported at the top of Fig. 5. The bias current I_b is generated off-chip by applying a square-wave voltage on a resistor connected in series to the Hall sensor. This hybrid setup is affected by parasitics and coupling effects. In particular, the high bumps shown in Fig. 5 (top) are due to parasitic capacitive coupling between bias nodes (A and B) and sensing nodes (C and D); this coupling is mainly due to the particular pin-out of the chip (i.e. pins connected to bias contacts are close to pins connected to sensing contacts). Although the output voltage suffers from high bumps at the beginning of the step response, the expected exponential response is clearly visible. From this result it is possible to estimate a time constant τ of 200 ns (extended uncertainty U=20 ns), which leads to C = 66 pF given R_{eq} = 3 kΩ. This is a reasonable value for a hybrid system made by discrete components.

B. Hall Sensing Element with Integrated Circuits

The step response of the Hall element integrated with conditioning circuits (case *b*) is shown at the bottom of Fig. 5. The bias current I_b is now generated on-chip by means of a high-compliance current mirror. Also in this case the measured voltage is not a pure exponential function since there are other residual dynamic effects acting on the response (e.g., the residual capacitive coupling between contacts and the ringing of the amplifiers which are underdumped second order systems). However, by fitting the output voltage with an exponential function it is possible to estimate an intrinsic time constant τ=12 ns (U = 3 ns), after de-embedding 4 ns as time response for each CMOS amplifier stage (which have 40 MHz bandwidth). The estimated time constant leads to a total capacitance C=4 pF (U=1 pF), which is in good agreement with the numerically estimated values of
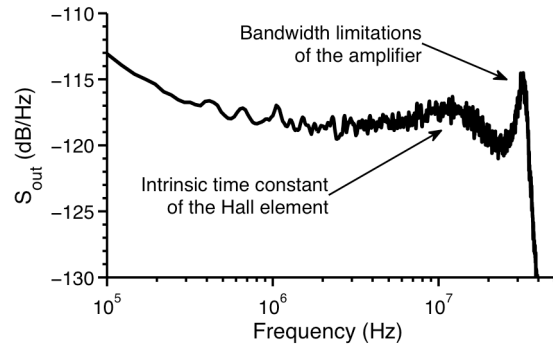

Fig. 6 Measured power spectrum of v_{out} for batch b only, when no current I is applied to the copper strip. The power spectrum confirms the time-domain measurement, showing a first cut-off frequency at 15 MHz (i.e. time constant τ=10 ns).

C_{acc}=0.9 pF and C_{in}=2 pF (those parameters are extracted from actual architecture and layout of the system).
In conclusion, both tests have been carried out in correspondence with operative conditions that activate a few parasitic dynamic effects, while the intrinsic parallel RC is fully excited. The experimentally obtained values for time constant and C, both for the implementation in which the capacitive load is maximized (case *a*) and for the sensor in which such a load is minimized (case *b*), are in agreement with numerical analysis, thus validating the model in Fig. 2-c and confirming that the bandwidth fundamental upper limit is set by the parallel RC behaviour. Parasitic dynamic effects are superimposed to such a fundamental response, and they degrade the actual bandwidth, as investigated in subsection IV-D.

C. Analysis in the Frequency Domain

A frequency analyses has been performed on batch b to further investigate the dynamic response of the Hall element. In this test, no current I has been applied to the strip, hence v_{OUT} is an amplified version of the thermal noise generated by the Hall element and the output amplifiers, only. The measured DC – 50 MHz output power spectrum S_{OUT} is shown in Fig. 6. This power spectrum can be interpreted as the frequency response of the entire current-measuring system; under the mild assumption of an algebraic relation between the measurand I and the magnetic field B. Interesting information is on the shape of the noise floor, which defines two important points: a first cut-off frequency around 15 MHz and a second cut-off frequency around 40 MHz. The former is related to a time constant of nearly 10 ns, in agreement with the intrinsic RC time constant of the Hall element measured in section IV-B, while the latter is related to bandwidth limitation of the output amplifiers. The measured power spectrum confirms the result of time-domain tests obtained in section IV-B.

D. Time Response to Actual Magnetic Transitions

The batch b has been tested also in the presence of an actual fast (but not instantaneous) time transition of magnetic excitation. In this test the Hall element is DC biased i.e., the current I_b is kept constant, so that output dynamics are related only to changes of magnetic field. We designed a simple voltage-to-current (V/I) converter based on a voltage follower and a 1-Ω power resistor (Fig. 7-a). The generated time-varying current $I(t)$ is monitored through the voltage drop across the power resistor, and then it flows through the metal strip on the top of the Hall element, generating the desired transition in the magnetic induction B. The designed V/I converter is characterized by a rise time of 210 ns, short but one order of magnitude longer than the fundamental response time estimated in section IV-B. Hence, the Hall element, as described by the model of Fig. 2-c, works in quasi-static regime as far as the intrinsic parallel RC is concerned. However, now the parasitic dynamic effects described by the black-box are fully triggered and will degrade the voltage response. This experiment provides useful information about these dynamic effects embedding the core of the sensor behaviour.

We acquired the voltage across the power resistor, translated it into the current I and fed it into the model of Fig. 2-c implemented in SPICE. The first version of the model takes into account the intrinsic parallel RC only. The predicted output voltage $\tilde{v}_{OUT}$ is then compared to the measured output voltage v_{OUT}. The voltage $\tilde{v}_{OUT}$ (Fig. 8, solid blue line) shows a quasi-instantaneous response to the measured current stimulus, as expected, (top of Fig. 8) but does not fit measurement data (red circle), since

the model neglects parasitic effects. Specifically, $\tilde{v}_{OUT}$ does not foresee the high bump opposite to the exponential transition. This mainly because the model still does not describe the parasitic emfs induced by time-varying magnetic induction (which must be modelled in the black box). In fact, when the model is made more realistic by inserting proper inductive equivalent elements in the black-box, in order to take into account parasitic emfs, then the predicted voltage (solid black line) accurately fits the measured data. In this case, the effect of parasitic emfs is well fitted by inserting a transformer in the black-box of Fig. 2-c. The measurand $I(t)$ flows into the primary winding generating an inductive effect on the secondary winding that is connected in series to the RC core of Fig. 2-c (secondary winding being 180 degree rotated). This test, when compared with that of Fig. 5-b, shows an example of degradation of the fundamental response when parasitic effects are triggered in realistic operation of the sensor. Suitable design methodologies must be employed in order to minimize the deviation from the fundamental bandwidth limit. For example, since the induced emfs are strictly related to the
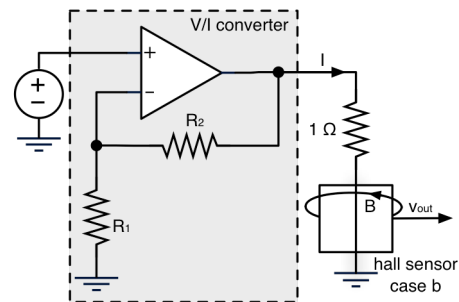

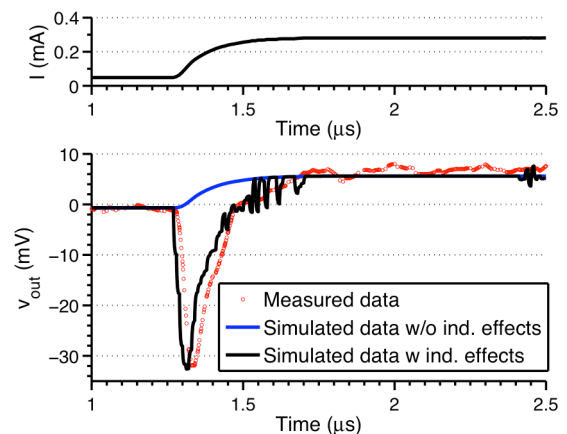Fig. 7 Measurement setup for time response to magnetic step.

Fig. 8 Measured response (red dots) to a step change of I (batch of case b) compared with simulated response given by the core model of Fig. 2-c (blue line) and with simulated response given by the enhanced model with inductive transformer (black line) Parameters used for simulation are $R=3\ k\Omega$, $C=4\ pF$, $L_{primary}= 10\ nH$, $L_{secondary}= 30\ nH$.

layout design of the implemented prototype, they can be reduced by proper geometrical redesign (e.g., minimizing the area described by connections from sensor to amplifiers).

V.   CONCLUSIONS

This paper experimentally investigated the bandwidth fundamental upper limit in Hall sensing elements. An equivalent electrical model describing the intrinsic dynamic response was defined. According to this model, an ad-hoc test allowed to experimentally characterized the intrinsic, fundamental time response of the Hall element in the time domain. The test was performed on two different batches of sensors, with same sensing element but different capacitive loads. The test demonstrated that capacitive effects define the intrinsic time response of the Hall sensor. This result fully agrees with numerical simulations and frequency-domain measurements, both reported in this manuscript.

A real-operation test was performed on one of the two batches, showing that actual time response of the Hall sensor is degraded by parasitic dynamic effects. Hence, suitable design methodologies are needed to achieve the fundamental time response. One of the parasitic effects degrading the sensor response, i.e. the generation of electromotive forces due to time-variant magnetic fields, has been investigated and an extension to the original model, which takes such effect into account, has been proposed.

REFERENCES

[1] L. Dalessandro, et al., "High-performance planar isolated current sensor for power electronics applications", IEEE Trans. on Power Electron. 22, pp.1682–1692. 2007.

[2] A. Patel, M. Ferdowsi, "Current Sensing for Automotive Electronics—A Survey", IEEE Trans. on Vehicular Technol. 58, pp. 4108–4119. 2008.

[3] P. Ripka, "Electric current sensors: a review", Meas. Science and Technol. 21, pp. 11-20. 2010.

[4] ACS709, "High-Bandwidth Current Sensor IC in Thermally Enhanced Package", Datasheet Rev.4, (2016).

[5] J. Jiang, W. J. Kindt, K. A. A. Makinwa, "A Continuous-Time Ripple Reduction Technique for Spinning-Current Hall Sensors", IEEE J. Solid-State Circuits. 49, pp. 1525–1534. 2014.

[6] CQ-3300, "High-speed response coreless current sensor", (2015).R.S. Popovic, "Hall Effect Devices", 2nd ed., Institute of Physics Publishing, 2004.

[7] R.S. Popovic, "Hall Effect Devices", 2nd ed., Institute of Physics Publishing, 2004.

[8] M. Crescentini, A. Romani, E. Sangiorgi, "Physical simulations of response time in Hall sensor devices", in: 2014 15th ULIS conf.m IEEE, 2014: pp. 89–92.

[9] SENTAURUS DEVICE User Guide, Version G-2012.06, Synopsis. Mountain View, CA.