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Setting up of a Floating-Gate test bench in a low noise environment to measure very low tunneling currents

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ABSTRACT
We propose and develop a complete solution to evaluate very low leakage currents in Non-Volatile Memories, based on the Floating-Gate Technique. We intend to use very basic tools (power supply, multimeter,...) but with a very good current resolution. The aim of this work is to show the feasibility of such measurements and the ability to reach current levels lower than the ones obtained by any direct measurement, even from high-performance devices. The key node is that the experiment is led in a very particular low-noise environment (underground laboratory) allowing to keep the electrical contacts on the device under test as long as possible. We have demonstrated the feasibility of this approach and obtained a very promising 10^{-17}A current level in less than two weeks.

Section: RESEARCH PAPER

Keywords: Flash memory; reliability; Floating-Gate Technique; leakage current; low noise

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1. INTRODUCTION

The Floating-Gate Technique (FGT) has been developed for many years [1], [2] in order to evaluate very low leakage currents through dielectrics. These currents are not accessible through direct electric characterization, even with high-performance analyzers [3], [4]. The principle of the technique lies in evaluating a slow temporal evolution of the electric charge of a MOS capacitance by an indirect measurement. The Floating-Gate device is a micro-electronic integrated test device. It is embedded in the scribe lines of a wafer and has to be probed under needles. In the context of Non Volatile Memories (NVM) reliability studies [5]-[9], the time range of one experiment is typically between several weeks and several months. To maintain the electrical contacts assured by needles over this long time, this technique requires protecting the probed device from external perturbations (principally mechanical vibrations and thermal variations). In a classical laboratory or industrial environment, it is difficult to set such a dedicated prober. For instance, this technique has been benched in the IM2NP characterization room [10] in a context of NVM Flash type reliability studies. On working days, the electrical contact of the needle can be hold, in best cases, over several hours and during winter holidays (empty laboratory), over a maximum of ten days. The development of this technique in a classical environment has been proposed in previous studies [11]. It requires a self-sustained prober, with compressed air network, in a thermalized artificial environment. This solution is technically and economically heavy (price of the hardware, space consuming, thermal control). If not impossible, it is very difficult to be developed. Thus, the main idea of our experimental platform lies in placing it in an underground room, naturally insulated from external perturbations. In the south of France near Apt, the very low noise underground laboratory, called LSBB ("Laboratoire Sous-Terrain à Bas Bruit") [12], offers such facilities. It consists in a set of horizontal galleries dug in the bedrock of Big Mountain, bordering the South Albion plateau. It was dedicated to be the

former cockpit shooting #1 of the French nuclear deterrent force, from 1973 to 1998. Rooms and galleries are shielded from electromagnetic waves, by concrete and massive slabs of steel. The depth varies between ground level down to 525 meters underneath the top of Big Mountain. The first peculiarity of this underground laboratory (compared to others) lies in its location in a Natural National Park, far from big communication ways (no highway, no railroad). The second appreciable peculiarity is its size: there are a lot of rooms of different sizes, each of them offering classical facilities (electrical and informatic network) for a scientific environment. The LSBB has been used by the National Institute of Universe (INSU) as a hydrogeological, geophysical (net of seismographs) and astronomical (muons detectors) observatory for a few years. It also allows to test microelectronic devices in a non-radiative environment. For our purpose, this laboratory is a very good environment since it naturally prevents from external perturbations (electromagnetic, mechanical, thermal variations) without any additional devices. It is important to notice that this laboratory is easy to access. Moreover the occupation fee for a single room is cheaper than a self-sustained marble table. Because the FGT only requires very basic electrical measurements (applying biases and acquiring currents), the technical hardware is standard and the probe station is a light one (35 kg). The entire experimental platform occupies around 2 square meters. This paper contains three major parts of development and a conclusion. First a background concerning NVM and FGT measurement is exposed, next the details of the experimental setup are presented, and finally the first results are shown and limitations of the measurements are discussed.

2. BACKGROUNDS

2.1. Non-Volatile Memories

The most widespread solution to enable semiconductor memories to be non-volatile - that is to say able to keep information without any power supply - is to use MOS transistors whose threshold voltage is shifted by a charge stored in an isolated gate above the channel [5]. The most common technology consists in adding a second gate between the gate and the channel of a classical MOS transistor. Flash memories are based on this principle. This second gate, made of conductor or semiconductor materials, can isolate charges to make the transistor threshold voltage variable. Most of the time, charges are injected through a dielectric, in general a thin silicon dioxide (SiO_2) layer, placed between the transistor channel and this second gate, as presented in Figure 1 (left). Lastly, the two gates of this "transistor" are also separated by a dielectric, most commonly a tri-layer stack oxide "Oxide/Nitride/Oxide" (ONO). Thus, the NVM elementary cell can be seen as a classical MOS transistor in series with a capacitor C_{pp} (Figure 1 right). The common electrode is called "Floating-Gate" (FG) because its electrical potential cannot be leaded by an external contact. It can store a charge while the top electrode of the capacitor becomes the "Control-Gate" (CG) of the cell.

Barrier transparency in the tunnel oxide, which can be electrically modeled by a current source *I*, allows the injection of charges in the floating gate, shifting the MOS transistor threshold voltage V_T according to (1), thus defining two different logical states:

$$V_T = V_{T0} - \frac{Q_{FG}}{C_{pp}} \quad (1)$$

where V_{T0} is the natural threshold voltage of the cell, Q_{FG} the charge amount in the Floating-Gate and C_{pp} the capacitance between the Control-Gate and the Floating-Gate.

A total quantity of elementary charges (electrons or holes) Q_{FG} is injected into the FG using an adequate set of biases, depending on technology [5]-[9]. These charges must be stored for a long time in the FG but they can escape from it through a damaged dielectric. According to (1), if charges are lost, the stored information will also be lost, since the two logical states cannot be distinguished anymore. A better understanding of physical phenomena responsible for the charge leakage, generally related to tunneling currents, is crucial to improve the whole quality of memory cells. This leakage current is not directly measurable in the NVM device.

The quality of this dielectric is a key for high reliability devices. That's why it is important to develop powerful methods allowing precise electrical characterizations of this dielectric. The main difficulty is to reach the very low current levels, responsible for such leakage, because they are not accessible through direct measurements, even with high-performance analyzers [3], [4]. Thus, some indirect measurement techniques have to be used. The Floating-Gate Technique is one of the most widely used methods.

2.2. Floating-Gate Technique (FGT)

The FGT is based on the use of a MOS capacitor and a MOS transistor in parallel [1], [2] as presented in Figure 2. It consists in a High-Voltage transistor whose gate is common with the Top Electrode of a large tunnel capacitor, denoted C_{tun}. This common gate plays the role of the Floating-Gate in a memory cell but is directly accessible to apply biases. The tunnel capacitor represents the injection zone of the memory cell. Indeed it has exactly the same process conditions as the injection region (oxide thickness, doping conditions…). Nevertheless, its area is much larger than that of the memory cell. Since the area ratio between the capacitor and the transistor is very high (around 1200:1) and the HV oxide is twice as thick as the tunnel oxide, the observed leakage is almost exclusively due to the tunnel capacitor. The FGT is based on the voltage measurement of the initially charged gate of the MOS capacitor, which is then disconnected from the external circuit during the experiment.

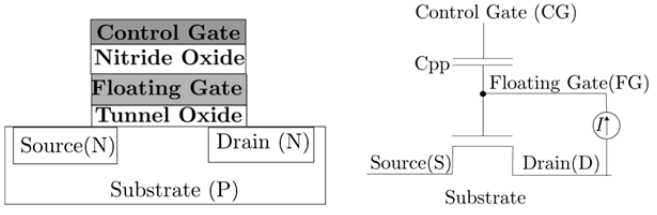

Figure 1. Schematic of a Flash-type NVM (left) and its electrical scheme (right).

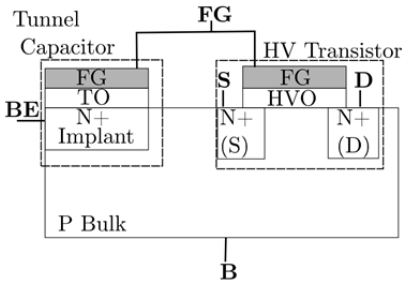

Figure 2. Floating-Gate test structure.

The measurement of this slowly decreasing gate voltage is performed indirectly through the measurement of the drain current of the transistor sharing its gate with the capacitor. This transistor "converts" the charge of the capacitor, and thus the gate voltage, in a measurable drain current. The temporal variation of this drain current is directly linked to the variation of the gate voltage and thus to its gate charge which is the same as the capacitor charge. Figure 3 depicts the full methodology to obtain the leakage current I_{leak} as a function of the Floating-Gate voltage V_{FG}. The drain current acquisition over time can be directly linked to a Floating-Gate voltage variation thanks to a preliminary $I_{DS}(V_{FG})$ measurement, illustrated in Figure 4.

The Floating-gate voltage is the image of the Floating-Gate charge Q_{FG}. It is extracted from the $C_{tun}(V_{FG})$ characteristics, presented in Figure 5, using (2):

$$Q_{FG} = C_{tun} \times V_{FG} \tag{2}$$

The leakage current I_{leak} is then the variation of this Floating-Gate charge Q_{FG} over time (3):

$$I_{leak} = -\frac{dQ_{FG}}{dt} \tag{3}$$

The acquisition of the drift of the drain current over very long time ranges is performed, keeping electrical contacts on the transistor (except on the Floating-Gate) during the whole experiment. As already detailed in the introduction, the main difficulty is to keep these electrical contacts for months: the longer the measurement, the lower the extracted current. The improvement presented here consists in developing a simple but very sensitive test bench. The low noise environment ensures the robustness against external perturbations.

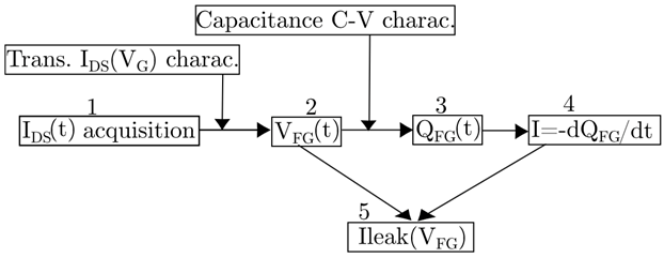

Figure 3. The five key points of Floating-Gate Technique methodology to extract leakage current.

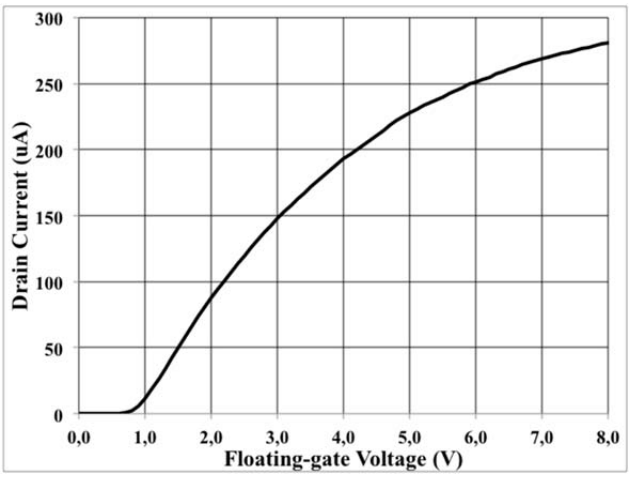

Figure 4. Preliminary $I_{DS}(V_{FG})$ measurement on the transistor from the Floating-Gate test structure.

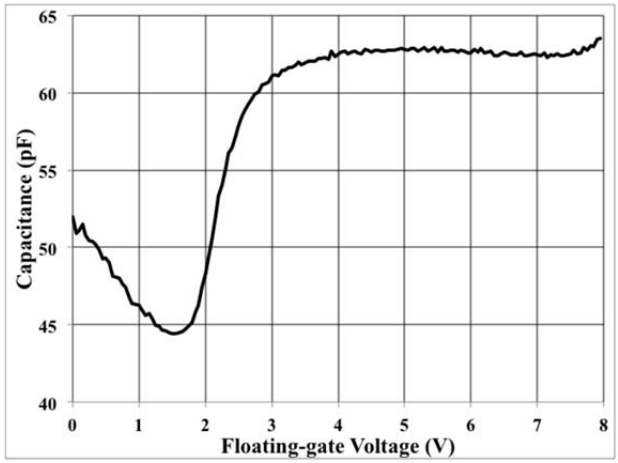

Figure 5. Preliminary $C_{tun}(V_{FG})$ measurement on the capacitor from the Floating-Gate test structure.

3. LOW NOISE ENVIRONMENT

The experimental platform has been installed at the end of the LSBB gallery, where the perturbations are supposed to be the smallest.

3.1. Proposed test bench

The test bench is composed of a classical probe station with 5 manipulators and needles. These manipulators are directly screwed on the probe station instead of being fixed by vacuum because the air pump would create undesired vibrations. The needles are then connected using standard coaxial cables to the power supply and the multimeter. An Agilent E3631A triple output DC power supply has been chosen because of its very good stability over time (0.1 % + 5mV after 12 months) [13]. Its cost is relatively limited and its use is widely spread, making the development of the remote controlling program easier. Concerning the drain current acquisition, the measured level is around 200 µA and a good resolution is needed to measure very low variations of this drain current. The Tektronix DMM4050 digital multimeter with a 6.5 digit and 100 pA resolution has been chosen [14]. Its cost is also relatively limited and it is easily programmable with any classical remote controlling software. The probe station is placed on a wood and iron workbench with an anti-vibration mat to absorb potential external perturbations. The power supply and the multimeter are placed on a separate support, also to reduce parasitic vibrations. The global test bench is shown in Figure 6. To avoid as much as possible any movement around the test bench, a fully remote controlled experiment is required.

Figure 6. Picture of the proposed test bench, embedded in the low-noise environment.

3.2. Remote controlling the experiment

LabVIEW from National Instruments has been chosen as a remote controlling software, which enables the use of the GPIB interface available on the devices to control them. A first program has been developed to perform the initial $I_{DS}(V_{FG})$ characteristics presented in Figure 4. The Floating-Gate of the transistor (and the capacitor) is then charged at the initial bias. The Floating-Gate needle is then lifted to let the capacitor slowly discharge through the dielectric.

The drain current acquisition (three current measurements, repeated each minute), controlled by a second program, is performed. Data are stored in a text file and saved regularly to be exported to an external computer located out of the low-noise environment.

4. PRELIMINARY MEASUREMENT RESULTS

4.1. Raw measurements

The first raw temporal acquisition of the drain current is shown in Figure 7. Noise currents appear randomly at different days. The relative RMS value is around 5 % of the mean drain current value (around 225 µA). It seems that there is an electrical external perturbation responsible for that. At this time we are not able to clearly explain the origin of this noise, but the ways to explore are linked to the hardware used in the setup experiment (PC, USB/GPIB adaptor…). It is probably an electrical phenomenon because during this first acquisition, there was a significant earthquake in Barcelonnette (small town in the "Alpes de Haute-Provence") located 50 km from the LSBB. This earthquake occurred on 07/04/2014 at 21h17min (local time), with a 5.1 magnitude on the Richter' scale [15]. All the seismographs in the LSBB have detected the earthquake, including the nearest of our platform (located at a few meters), but measurements have not been perturbed as can be seen in the zoom of the measurements presented in Figure 8. That is to say the mechanical contacts between the points and the electric pads of the tested device seem to be reliable for high frequency perturbations. The high frequency noise observed in measurements is visible because when noise occurs, the three consecutive measurements at the same minute are different. That is to say the current noise is at higher frequency than the time resolution measurement of the DMM4050 multimeter.

To further explore the reason of this noise on the drain current acquisition, the spectrum of this noise current could be studied. Nevertheless, this noise current has been removed by increasing the number of successive acquisitions while drastically reducing the number of measurements over time (six

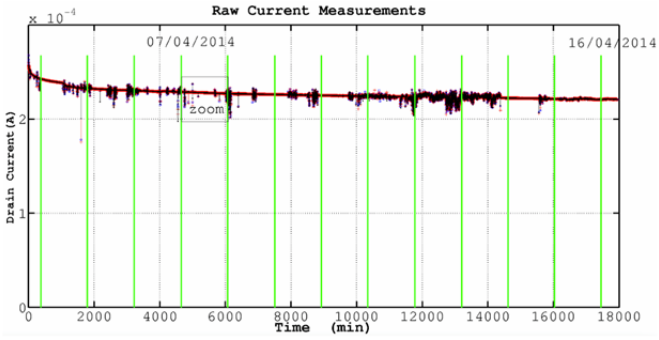

Figure 7. Raw drain current acquisition. Each vertical line denotes a change of day (midnight), from 03/04/2014 to 16/04/2014. The initial gate voltage of the capacitor is 7V here and the Drain-Source bias is V_{DS} = 0.1 V.

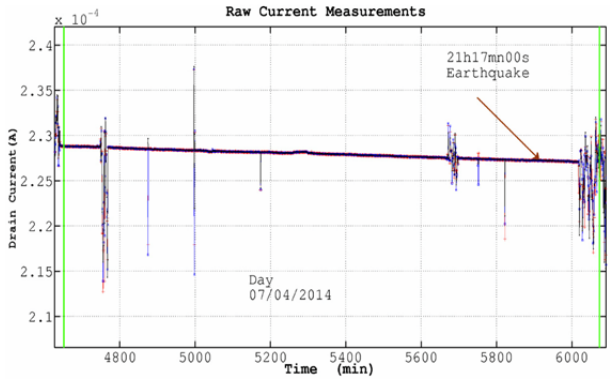

Figure 8. Raw drain current acquisition during the Earthquake day 07/04/2014. (Same legend than Figure 7).

successive acquisitions every hour instead of three successive acquisitions every minute previously) and with a higher integration time (2 seconds instead of some tens of milliseconds previously). The improvement can be observed in Figure 9.

4.2. Estimation of the global sensitivity of the measurement protocol

Figure 10 presents the results of measured drain currents (I_{DS}), on a discharged capacitor, for around 400 measurements, each separated by 20 minutes. Three drain polarizations (V_{DS} = 0.1 V ; V_{DS} = 0.3 V and V_{DS} = 0.5 V) have been investigated to eventually detect a sensitivity due to the drain polarization. The statistical means and standard deviation of the drain current extracted from Figure 10 are reported in Table 1.

These results are coherent with the ones obtained when the multimeter DMM4050 is not connected (empty measurements)

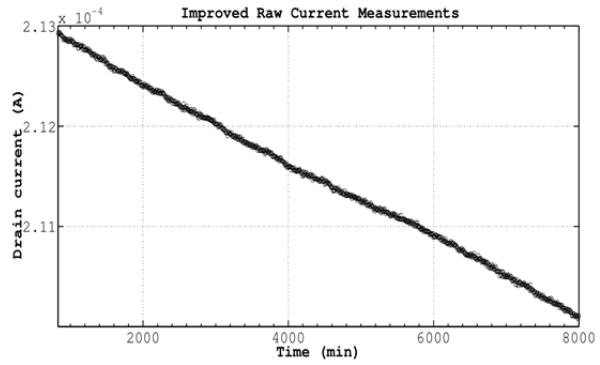

Figure 9. Improved raw current measurements, using the new acquisition protocol.

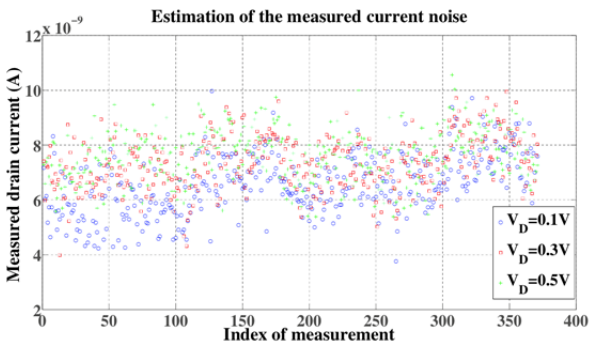

Figure 10. Statistical global current sensibility estimation.

Table 1. Statistical mean and standard deviation (STD) of the measurements presented in Figure 10.

V_{DS} (V)	0.1	0.3	0.5
Mean (nA)	6.54	7.34	7.62
STD (nA)	1.1	0.97	0.95

to any device and the ones given by the constructor [14]. The lowest significant variation of the current can be estimated around 1 nA while the lowest significant current measurable can be evaluated around 8 nA. For the following process of extraction of the leakage current, those values are not critical. However it will be important to take them into account at the end of the retention time - for very low values of I_{DS}. Indeed, the derivation process of the charge is impacted by the precision in the measurements.

4.3. Low leakage current extraction

From non-noisy measurements presented in Figure 9 and the preliminary characteristics, the total electrical charge in the floating gate is extracted according to the FGT methodology (Figure 3). The numerical derivative (or a local fitting) gives the leakage current assuming that the numerical variations taken into account are greater than the STDs given in Table 1. It is clearly the case for the level of currents involved in this section. Then, it is also possible to plot this leakage current versus the Floating-Gate voltage as presented in Figure 11. We can first notice in Figure 11 the continuity between the two methods (direct measurements and FGT extraction) at high current levels around 6.5 V. For low levels, the best result obtained with a classical Agilent HP4156 (with a long integration time and Force/Sense cables) is around 10^{-15} A. However, using the FGT, in less than two weeks two additional decades have been reached with a level around 10^{-17} A. To our knowledge, keeping electrical contacts over such a long time in a classical laboratory has needed very heavy equipment with extracted current levels over 10^{-17} A after a maximum of 45 days [11]. Moreover, the resolution obtained for the leakage current can be statistically estimated. A first evaluation is done thanks to the three successive acquisitions performed during the experiment. Considering these three measurements as three independent acquisitions, the difference between the maximum value and the minimum value of these three independent extractions of the leakage current is plotted in Figure 12.

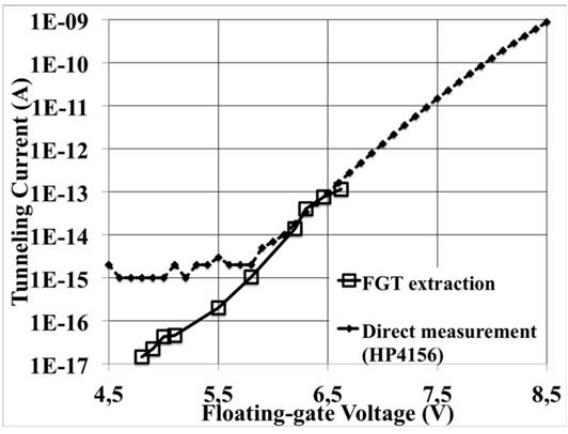

Figure 11. Comparison between direct measurement and Floating-Gate Technique extraction.

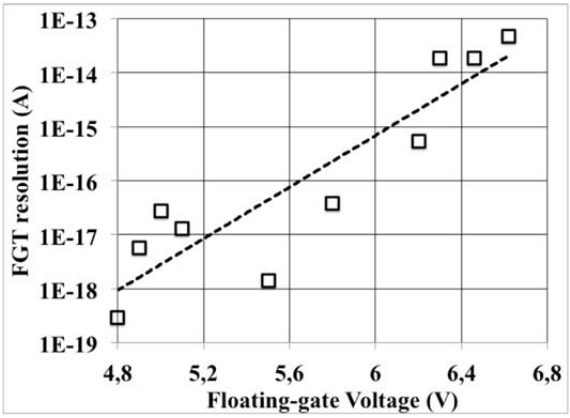

Figure 12. Evaluation of the Floating-Gate Technique resolution using three independent acquisitions during a single experiment.

We notice that the resolution of the extraction improves drastically during the experiment. Indeed, for relatively high current level extraction the resolution is around 10^{-14} A but when extracting lower current levels, the resolution decreases down to around 10^{-19} A. It is one of the main known advantages of the Floating-Gate Technique to have a resolution improving with time. This is a promising preliminary result, awaiting better results from further measurements which can be performed over months in the proposed specific environment.

5. CONCLUSION AND PERSPECTIVES

Following the very classical protocol of the Floating-Gate Technique, the feasibility of an approach with a very simple test bench, embedded in a very low-noise environment has been proven. In less than two weeks a leakage current lower than the minimum directly measurable one with any classical tool has been extracted. The first improvement performed on the proposed experimental platform has been to find the reasons of the electrical noise and to reduce it by modifying the acquisition methodology. The natural perspective of this work is the continuation of the drain current acquisition in a long-time range. It also requires a reliable and reproducible process to extract leakage current from the charge versus time evolution. This experimental work should also be completed by a theoretical and numerical approach that would allow to theoretically and numerically model the loss of charges through the oxide. The developed FGT can also be reproduced on oxides, previously damaged with conditions close to those used in NVM products, to study the reliability of such memory cells.

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