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Very low tunneling current measurements using the Floating-Gate technique in a very low-noise environment

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Abstract – **In this paper we propose and develop a complete solution to measure very low tunneling currents in Non-Volatile Memories, based on the Floating-Gate technique. We aim at using very basic tools (power supply, multimeter, ...) but still having a very good current resolution. The key node of our solution is that the experiment is led in a very particular low-noise environment (underground laboratory) allowing to keep the electrical contacts on the device under test as long as possible. The aim of this work is to show both the feasibility of such measurements and the ability to reach current levels lower than the ones obtained by any direct measurement, even from high-performance devices such as HP4156 or Agilent B1500 with atto-sense and switch unit (ASU). We have demonstrated the feasibility of this approach and obtained a very promising $10^{-17}A$ current level in less than two weeks.**

I. INTRODUCTION

Flash memory cells are based on the floating gate technology principle [1]. The most widespread solution to enable semiconductor memories to be non-volatile, that is to say their ability to keep information without any power supply, is to use MOS transistors whose threshold voltage is shifted by a charge stored in an isolated gate above the channel. Floating gate technologies consist in adding a second gate between the gate and the channel of a classical MOS transistor. This second gate, in conductor or semiconductor materials, can isolate charges to make the transistor threshold voltage variable. Most of the time, charges are injected through a dielectric, in general Silicon dioxide SiO_2, placed between the floating gate and the transistor channel, as presented in Fig. 1. Last, the two gates of this "transistor" are also separated by a dielectric, most commonly a tri-layer stack oxide "Oxide/Nitride/Oxide" (ONO). Thus, the Flash elementary cell, constituted by a floating gate transistor called "state transistor", can be seen like a classical MOS transistor whose gate would be in series with a capacitor C_{pp}. This gate which is called "Floating Gate" (FG) can now store a charge while the second electrode of the capacitor becomes the "Control Gate" (CG) of the cell.

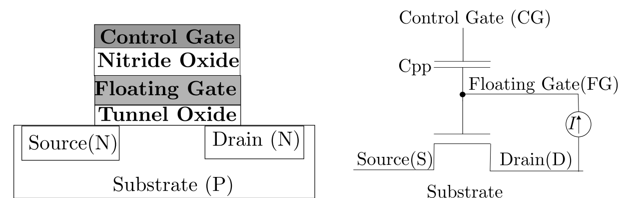

Fig. 1. Schematic of a floating gate structure (left) and its electrical scheme (right).

Barrier transparency in the tunnel oxide, which can be electrically modeled by a current source I, allows the injection of charges in the floating gate, shifting the MOS transistor threshold voltage V_T according to equation (1):

$$V_T = V_{T0} - \frac{Q_{FG}}{C_{pp}} \quad (1)$$

where V_{T0} is the natural threshold voltage of the cell, Q_{FG} the charge amount in the floating gate and C_{pp} the capacitor between the control gate and the floating gate.

Q_{FG} quantity is injected into the floating gate by using an adequate set of biases, depending on technology (Flash or EEPROM) [2, 3, 4, 5]. Memory cell reliability, defined as the capability of said device to function over time, is a major issue for manufacturers and can be related to many parameters such as process and using conditions. Indeed, unceasing device scaling, decrease of dielectric thicknesses around the floating gate and high voltages applied on cells are many parameters altering memory reliability [6].

Thus, dielectrics' quality is a major issue due to their antagonistic roles: avoiding electric charge leakage currents during retention phase while being transparent enough during programming steps. A better understanding of these leakage currents is crucial to improve the whole quality of

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our memory cells, that's why we have to develop powerful methods to reach very low current levels.

The Floating Gate Technique is one of those methods, exposed in the next section. Using this method needs i) to protect the wafer from mechanical (vibrations) perturbations and ii) (very) long time acquisition. In a classical laboratory environment, those two constraints are generally not easy to deal with. Indeed, they lead to use, for a very long time, huge, heavy and very expensive probers (mechanically insulated by air shocks), that is often economically not possible. The main idea of our experimental platform, exposed here, consists in developing a "cheap" platform. The mechanical insulation is "naturally" done by the very peculiar environment of the LSBB Laboratory located in Apt (South of France). The aim of this paper is to expose very first results, show the feasibility of the measurements and discuss the possible improvements.

II. FLOATING-GATE TECHNIQUE (FGT)

Most of the electrical measurements developed to characterise semiconductor devices and especially Non-Volatile Memories are based on current measurements. Indeed, to study a major reliability aspect of these NVM we have to evaluate the very low-level leakage currents responsible for the charge loss during the retention phase. Nevertheless, these currents are not accessible through direct measurements, even with high-performance analyzers [7], so we have to use some indirect measurement techniques to reach lower level currents. One of the most widely used technique is the "Floating-Gate Technique" (FGT), based on the use of a MOS capacitor and a MOS transistor in parallel [8, 9].

A. Floating-Gate test structure

The Floating-Gate test structure, presented in Fig. 2, consists in a large High-Voltage transistor whose gate is common with the Top Electrode of a large tunnel capacitor. This common gate plays the role of the Floating-Gate in a memory cell but is directly accessible to apply biases. Since the area ratio between the capacitor and the transistor is very high (around 1200:1) and the HV oxide is twice as thick as the tunnel oxide, so the observed leakage is almost exclusively due to the tunnel capacitor.

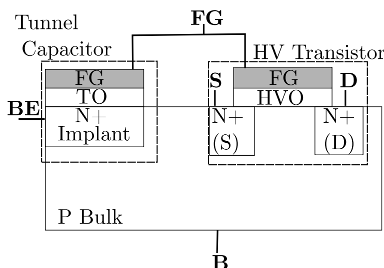

Fig. 2. Floating-Gate test structure.

B. Floating-Gate Technique methodology

The Floating-Gate Technique (FGT) is based on the measurement of the voltage of an initially charged gate of a MOS capacitor, which is then disconnected of the external circuit during the experiment to slowly decrease. The measurement of this gate voltage is performed indirectly through the measurement of the drain current of the transistor sharing its gate with the capacitor. This transistor "converts" the charge of the capacitor, and thus the gate voltage, in a measurable drain current. The temporal variation of this drain current is directly linked to the variation of the gate voltage and thus to its gate charge which is the same than the capacitor charge. Fig. 3 depicts the full methodology allowing to obtain the tunneling current I_{tun} as a function of the Floating-Gate voltage V_{FG}.

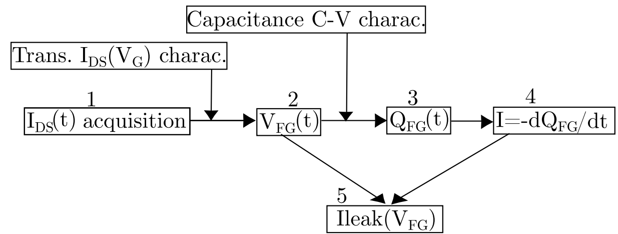

Fig. 3. The five key points of Floating-Gate Technique methodology to extract leakage current.

The drain current acquisition over time can be directly linked to a Floating-Gate voltage variation thanks to a preliminary $I_{DS}(V_{FG})$ measurement, illustrated in Fig. 4.

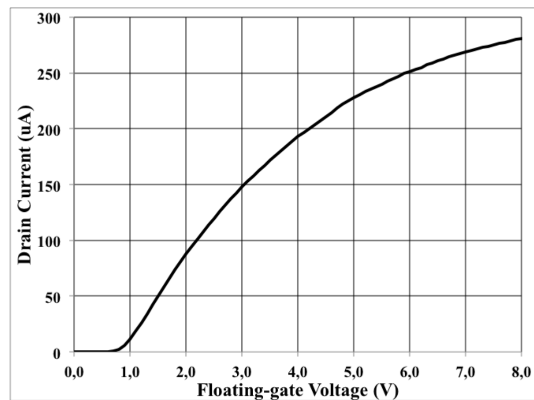

Fig. 4. Preliminary $I_{DS}(V_{FG})$ measurement on the transistor from the Floating-Gate test structure.

This Floating-gate voltage is the image of the Floating-Gate charge Q_{FG}, extracted from the $C_{tun}(V_{FG})$ characteristics, presented in Fig. 5, using equation (2):

$$Q_{FG} = C_{tun} \times V_{FG} \quad (2)$$

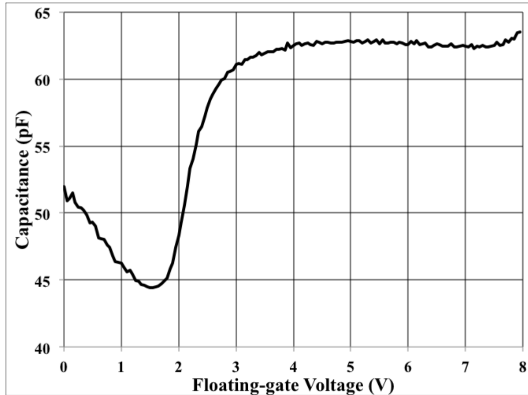

Fig. 5. Preliminary $C_{tun}(V_{FG})$ measurement on the capacitor from the Floating-Gate test structure.

The leakage current I_{tun} is then the variation of this Floating-gate charge Q_{FG} over time (3):

$$I_{tun} = -\frac{dQ_{FG}}{dt} \tag{3}$$

To reach very low-level currents, we have to acquire the drift of the transistor drain current over very long time, keeping applied biases on the transistor (except on the Floating Gate) during the whole experiment. The main difficulty is to keep the electrical contacts on the device under test for days, weeks or even months, knowing the longer the measurement, the lower the extracted current. When using classical probe stations, it is difficult to keep electrical contacts for more than a few days due to the ambient vibrations [10]. Electromagnetic perturbations also disturb the experiment due to the very slow drift of the drain current we have to measure. All the existing solutions to enable a long drain current acquisition lead to very heavy and expensive test bench that we propose to avoid in our study. The improvement consists in developing a cheap but very sensitive test bench, embedded in a particular environment.

III. LOW-NOISE ENVIRONMENT

To reach very low levels of electrical and mechanical noises, we have first chosen a specific test environment with a very low electromagnetic noise and a very low vibration level, allowing to use a very simple test bench.

A. A specific test environment: the Low Noise Underground Laboratory of Rustrel

The Low Noise Underground Laboratory in Rustrel Pays d'Apt (South of France) is a set of horizontal galleries dug in the bedrock of Big Mountain, bordering South Albion plateau. It was dedicated to be the former cockpit shooting # 1 of the French nuclear deterrent force, from 1973 to 1998. It was built to resist a nuclear weapon assault. It allows access to different rooms (for a total of $14,000\text{m}^2$) along 3.7 km, in a rock cover varying from 30 to 519 m under the Surface topography. Rooms and galleries are shielded (electromagnetic waves), by concrete and massive steel shields. This peculiar environment is now used by the National Institute of Universe (INSU) as a hydrogeological, geophysical (net of seismographs) and astronomical (muons detectors) observatory since few years. It also allows to test microelectronic devices in a non radiative environment. For our purpose, this laboratory is the "perfect environment" since it allows to avoid electromagnetic and mechanical perturbations during a very long time range. Our platform has been installed at the end of the gallery, where the perturbations are supposed to be the smallest.

B. Proposed test bench

Our test bench is composed of a classical probe station with 5 manipulators and needles. These manipulators are directly screwed on the probe station instead of being fixed by vacuum because the air pump would create undesired vibrations. The needles are then connected using standard coaxial cables to the power supply and the multimeter. We have chosen an Agilent E3631A triple output DC power supply because its stability over time is very good ($0.1\% + 5\text{mV}$ after 12 months) to bias the drain of the transistor during the whole experiment duration [11]. Its cost is relatively limited and its use is widely spread, making the development of the remote controlling program easier, which will be presented in the next section. Concerning the drain current acquisition, the measured level is around $200\mu\text{A}$ and we need a good resolution to measure very low variations of this drain current. We have chosen a Tektronix DMM4050 digital multimeter with a 6.5 digit and 100pA resolution [12]. Its cost is also relatively limited and it is easily programmable with any classical remote controlling software. The probe station is placed on a wood and iron workbench with an anti-vibration mat to absorb potential external perturbations. The power supply and the multimeter are placed on a separate support, also to reduce parasitic vibrations.

C. Remote controlling the experiment

To avoid as much as possible any movement around the test bench, we had to develop a fully remote controlled experiment. As a remote controlling software, we have chosen *Labview* from *National Instruments* which enables to use the GPIB interface available on our devices to control them. We have first developed a program to perform the initial $I_{DS}(V_{FG})$ characteristics as described in Fig. 3. Then we manually pre-charge the floating gate of the transistor (and the capacitor) at the initial bias and lift the needle connected to this floating gate to let the capacitor slowly discharge. We can begin the acquisition of the drain current drift, performed by a second program. This one controls the multimeter and performs three current measurements, repeated each minute. The data are stored in a

text file and saved regularly to be exported to an external computer located out of the low-noise environment. Thus we achieve our goal of having a very-low noise environment, without any physical interaction in the neighbourhood of the experiment.

IV. VERY FIRST MEASUREMENTS

A. *Raw measurements*

The extraction methodology requires two preliminary characteristics, the $I_{DS}(V_{FG})$ characteristics of the transistor and the C-V curve of the capacitor, which have already been presented in Figures 4 and 5, respectively. The C-V measurements have been performed first on the whole wafer to check the very low dispersion on the wafer. Then the $I_{DS}(V_{FG})$ characteristics is performed directly in the low-noise environment. The first raw temporal acquisition of the drain current drift is shown in Fig. 6.

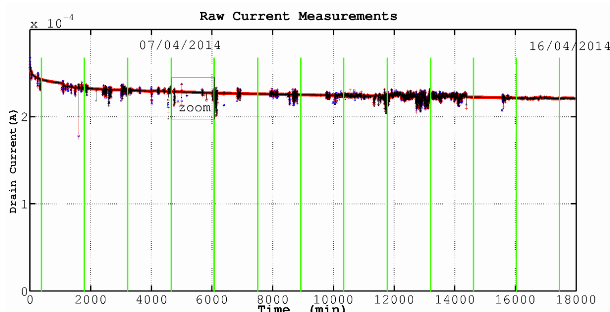

Fig. 6. Raw drain current acquisition. Each vertical line denotes a change of day (midnight), from 03/04/2014 to 16/04/2014. The initial potential of the capacitor is $7V$ here and the Drain-Source bias is $V_{DS} = 0.1V$

Noise currents appear randomly at different days. The relative RMS value is around 5% of the mean drain current value (around 225μA) from Fig. 6. It seems that there is an electrical external perturbation responsible of that. At this time we are not able to clearly explain the origin of such a noise, but the ways to explore are linked to the hardware used in the setup experiment (PC, USB/GPIB adaptator, . . .). We think it's an electrical phenomenon because during this first acquisition, there was a significative earthquake at Barcelonnette (little town in the "Alpes de Haute-Provence") located at 50km of the LSBB. This earthquake occurred on 07/04/2014 at 21h17min (local time), with a 5.1 magnitude in Richter's scale [13]. All the seismographs in the LSBB have detected the earthquake, including the nearest of our platform (located at a few meters), but our measurements have not been perturbed as can be seen in the zoom of the measurements proposed in Fig. 7.

That is to say the mechanical contacts between the points and the electric pads of the tested device seem to be reliable for high frequency perturbations. The noise observed in our measurements is also at "high" frequency. It

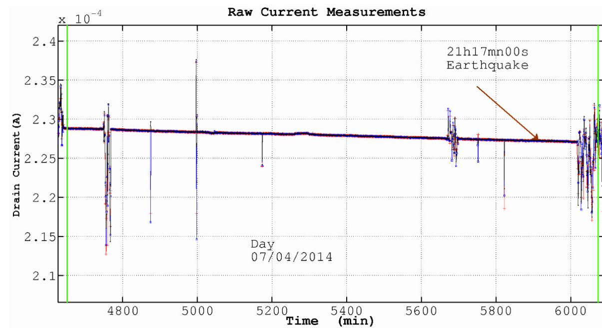

Fig. 7. Raw drain current acquisition during the Earthquake day 07/04/2014. (Same legend than Fig. 6)

is visible because when noise occurs, the three consecutive measurements at the same minute are different. That is to say the current noise is at higher frequency than the time resolution measurement of the DMM4050 multimeter. To further explore the reason of this noise on our drain current acquisition, we could search the spectrum of this noise current. Nevertheless, we succeeded in almost removing this noise current by increasing the number of successive acquisitions while drastically reducing the number of measurements over time (six successive acquisitions every hours instead of three successive acquisitions every minutes previously) and with a higher integration time (2 seconds instead of some tens of milliseconds previously). The improvement can be observed in Fig. 8.

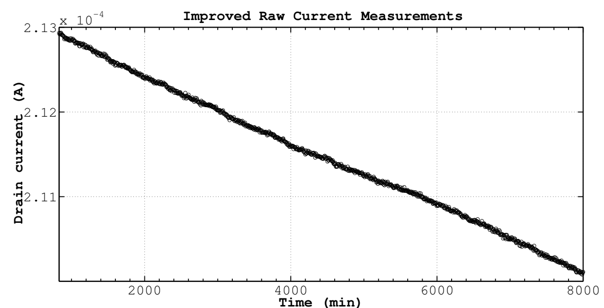

Fig. 8. Improved raw current measurements, using the new acquisition protocol.

B. *Low leakage current extraction*

To extract the first order of magnitude of the leakage current obtainable, we choose, first, non noisy measurements. Then, with the preliminary characteristics , it is possible to extract the total electrical charge in the floating gate. The numerical derivative (or a local fitting) gives the leakage current. It is also possible to plot it versus the floating gate voltage as presented in Fig. 9.

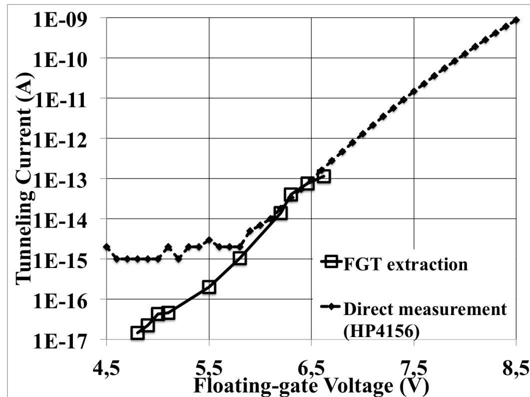

Fig. 9. Comparison between direct measurement and Floating-Gate Technique extraction.

The best results we can obtain with a classical Agilent HP4156 (with a long integration time and Force/Sense cables) is around 10^{-15}A but in less than two weeks, we have obtained with our experiment two additional decades with a level around 10^{-17}A. The resolution of our method can be estimated by extracting this low current level for a large number of experiments on the same device. We can make a first evaluation of this resolution thanks to the three successive acquisitions we have performed during our experiment. If we consider these three measurements as three independent acquisitions, we can plot in Fig. 10 the difference between the maximum value and the minimum value of these three independent extractions of the leakage current. We can notice that the resolution of our extraction improves drastically during the experiment. Indeed, for relatively high current level extraction the resolution of our method is only around 10^{-13}A but when we extract lower tunneling current levels (for lower floating-gate voltages), the resolution decreases down to around 10^{-19}A. It is one of the main advantages of the Floating-Gate Technique to have a resolution improving with time.

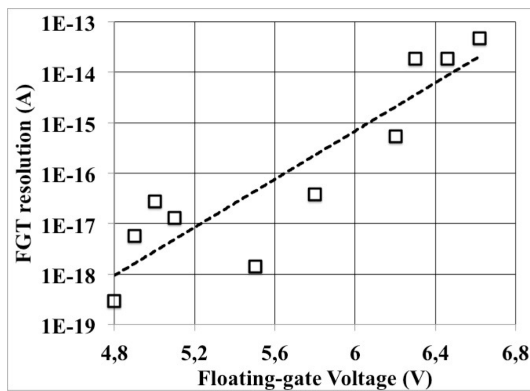

Fig. 10. Evaluation of the Floating-Gate Technique resolution using three independent acquisitions during a single experiment.

Moreover, we can also notice in Fig. 9 the continuity between the two methods at higher current levels around 6.5V. This is a promising preliminary result, awaiting better results from further measurements.

V. CONCLUSION

Following the very classical protocol of the Floating Gate measurement, we have proven the feasibility of our approach with a very cheap test bench, embedded in a very low-noise environment. In less than two weeks we have been able to extract a leakage current lower than the minimum directly measurable with any classical tool (Agilent 4156) or even with advanced tools (Agilent B1500). The immediate way to improve our method lies in finding the reasons of the electrical noise and reducing it by applying the adequate solutions.

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