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Digital reconstruction stage of the FBD ΣΔ-based ADC architecture for multistandard receiver

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***Abstract* – This paper presents the design of a digital reconstruction stage for a frequency band decomposition (FBD)-based analog-to-digital converter (ADC) architecture for digitizing multistandard receiver signals. The proposed FBD-based ADC architecture is flexible with programmable parallel branches composed of discrete time (DT) 4th order single-bit ΣΔ modulators. The mixed baseband architecture uses a single non programmable anti-aliasing filter (AAF) avoiding the use of an automatic gain control (AGC) circuit. System level analysis proved that proposed FBD architecture satisfies design specifications of the proposed software defined radio (SDR) receiver. In this paper, the authors focus essentially on the reconstruction stage design for UMTS use case while discussing digital stage processing and performances.**

I. INTRODUCTION

Software defined radio (SDR) is a state-of-the-art technology solution of software radio concept, first introduced by Mitola [1]. SDR was proposed by scientists to achieve a feasible multistandard receiver. To ensure software reconfigurability, received signals must be digitized as near as possible to the antenna in order to reduce analog circuitry. This leads to inscrease design constraints on the analog-to-digital converter (ADC). In fact, in the litterature, there is no fully integrated ADC that covers different coexisting wireless and mobile standards from narrowband to wideband channel with different required dynamic ranges [2]. To deal with this problem, the authors take advantage of parallel architectures of ΣΔ modulators that ensure high accuracy, in terms of dynamic range, while extending conversion bandwidth.

Parallel architectures have become an attractive solution for analog-to-digital conversion. There are three main parallel architectures in the literature, as the Hadamard modulated parallel architecture (ΠΣΔ) [3], the time-interleaved architecture (TIΣΔ) [4], and the frequency band decomposition (FBD) architecture [5]. In this paper, the authors choose FBD architecture because unlike ΠΣΔ and TIΣΔ architectures, FBD architecture is not sensitive to gain and offset mismatches [6]. In the FBD architecture, the parallel ΣΔ modulators are band-pass (BP) and each one converts a part of the total input signal band. A novel flexible FBD architecture based on 4th order single-bit ΣΔ modulators was proposed in [7]. The solution presents programmable parallel branches with different sub-bandwidths, where only some branches are activated according to the selected standard. In this paper, to design and test the FBD ΣΔ-based ADC, the authors propose a design of the digital reconstruction stage based on demodulation.

In section II, the design of an FBD ΣΔ-based mixed baseband stage with a unique passive AAF ahead intended for an SDR receiver is presented. Section III deals with the digital reconstruction stage of the FBD ΣΔ-based ADC. The two approaches existing in the literature which corresponds to direct reconstruction and demodulation-based reconstruction are discussed [5]. A digital reconstruction stage with demodulation design for UMTS use case is proposed. Simulation results of the FBD ΣΔ-based ADC model on Matlab/Simulink are presented in section IV. Finally, section V draws some conclusions.

II. FLEXIBLE FBD ΣΔ ARCHITECTURE DESIGN

Considering system level specifications from the standards, conventional mixed baseband stage design [7] has been modified to adapt it to parallel ΣΔ modulators architecture. FBD architecture design is therefore presented in this section.

The multistandard receiver processes E-GSM, UMTS and IEEE802.11a communication signals [7]. A hybrid homodyne/low-IF architecture was proposed in [8] for the SDR front-end. An RF filter selects the received signals. Afterward, they are amplified by a low-noise amplifier (LNA). Then, on the one side, the UMTS and IEEE802.11a signals are down-converted by the mixer to

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baseband frequencies. On the other side, the E-GSM signals are down-converted to a low intermediate frequency of 100 kHz to ovoid flicker noise disturbance.

A. Mixed baseband architecture

The mixed baseband stage, presented in Fig. 1 [7], follows the mixer which is controlled by the local oscillator (LO). The mixed baseband stage is composed of a single passive low-pass anti-aliasing filter (AAF) that precedes the FBD ΣΔ-based ADC. There is no need for automatic gain control (AGC) circuit before the ADC stage since the AAF filters only E-GSM blockers that are outside the IEEE802.11a bandwidth [8]. The M parallel single-bit ΣΔ modulators outputs are combined in the digital reconstruction stage that follows the ΣΔ modulators to reconstruct the final output.

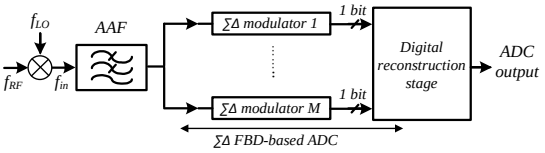


Fig. 1. FBD ΣΔ-based mixed baseband stage.

B. Flexible FBD ΣΔ architecture

The authors in [7] started from SDR receiver specifications in terms of channel bandwidths and ADC required dynamic ranges for the chosen communication standards. The designed discrete-time (DT) FBD ΣΔ architecture for ADC stage was proposed in [7]. The design realizes a trade-off between increasing the sampling frequency while still operating in discrete time and increasing the number, M, of parallel branches regarding a low-complexity goal, or increasing ΣΔ modulators orders while keeping them stable. Thus, an FBD ΣΔ architecture which is composed of 6 programmable parallel branches was proposed in Fig.2.

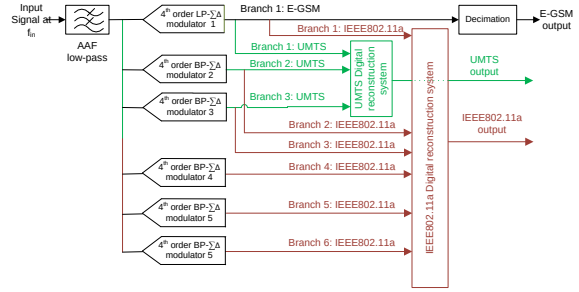


Fig. 2. Designed FBD ΣΔ-based ADC architecture.

According to the communication standard signal, only needed branches from the whole architecture are activated. Each branch is composed of a DT 4th order single-bit quantizer ΣΔ modulator. The ΣΔ modulator order is defined as the number of integrators or resonators, *k*, for low-pass (LP) and band-pass (BP) ΣΔ modulators, respectively. In this paper, since the designed FBD architecture is composed of both LP and BP ΣΔ modulators, the authors designate *k* as ΣΔ modulator order [5].

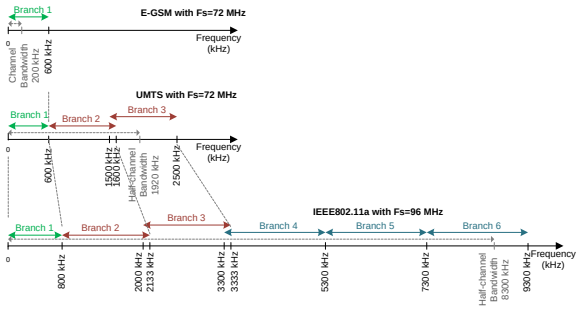


Fig. 3. Branch frequency division plan.

Besides, the used ΣΔ modulators in the FBD architecture are based on non unitary signal transfer function (NU-STF) that permits dealing with stability problems and recovering input signal dynamic range [7]. The branch bandwidths are different and the sampling frequencies vary from radio communication standard to another in order to optimize the flexible FBD ΣΔ architecture while fulfilling the theoretical required dynamic ranges. The branch bandwidth and the sampling frequency according to the chosen standard are given by the branch frequency division plan presented in Fig. 3.

III. DIGITAL RECONSTRUCTION STAGE

In the literature, there are two main approaches to reconstruct output signal from the parallel ΣΔ modulators outputs while ensuring required dynamic range [5]. For the first solution, the ΣΔ modulators outputs are directly processed using band-pass filters then the selected signals are decimated. However, the second solution demodulates each ΣΔ modulator output signal by converting it to baseband frequencies, then it is decimated before being processed by a low-pass filter. It was shown in [5] that the digital reconstruction with direct processing presents high complexity due to high required BP filters orders and operating sampling frequencies. The digital reconstruction with demodulation requires lower LP filters orders and operating sampling frequencies. Consequently, in this paper, the authors proceed to digital reconstruction with demodulation whose architecture is explained in the sub-section A. In sub-section B, the authors take the UMTS as a use case of the FBD ΣΔ architecture that is only composed of the first three parallel branches as presented in Fig. 2.

A. Digital reconstruction with demodulation

The digital reconstruction architecture with demodulation is presented by Fig. 4. In this digital processing, the BP ΣΔ modulators output signals are first brought to baseband by processing a complex demodulation. This operation consists in multiplying modulators outputs by the complex sequence $m_k[n]$ as given by (1) where f_{c_k} is the central frequency of the k^{th} branch bandwidth and *n* is positive integer.

$$m_k[n] = e^{-2i\pi f_{c\_k} n} \quad (1)$$

After complex demodulation operation, since the ΣΔ

modulators oversample input signals [2], it is mandatory to proceed to decimation and filtering operations. Hence, each demodulated signal is decimated in order to decrease its sampling frequency and bring it to Nyquist frequency defined as the double of the channel bandwidth. The global decimation factor is equal to the global oversampling ratio, *OSR*, defined as the sampling frequency, F_S, out of the Nyquist frequency. Then, each demodulated and decimated signal is processed by a low-pass filter that selects branch bandwidth before being remodulated. The remodulation operation consists in frequency up-converting each baseband signal around the corresponding branch central frequency at the Nyquist frequency. Finally, the output signals of the parallel branches are recombined to form the output signal of the FBD architecture. For the first branch that operates with a LP-ΣΔ modulator, there is no need to demodulate and remodulate as shown in Fig. 4.

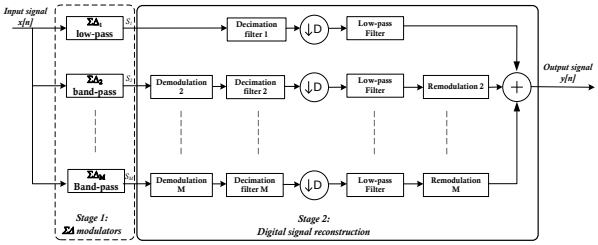


Fig. 4. Digital reconstruction with demodulation of the FBD architecture.

B. Proposed FBD based ADC architecture

The model of the FBD ΣΔ -based ADC architecture with demodulation-based digital reconstruction is designed using Matlab/Simulink as presented by Fig. 5. The model corresponds to the use case of the FBD architecture intended for UMTS signals. It is composed of 3 branches in parallel which are operating at a sampling frequency equal to 72 MHz with branches bandwidths as explained by the branch frequency division plan for UMTS signals presented by Fig. 3.

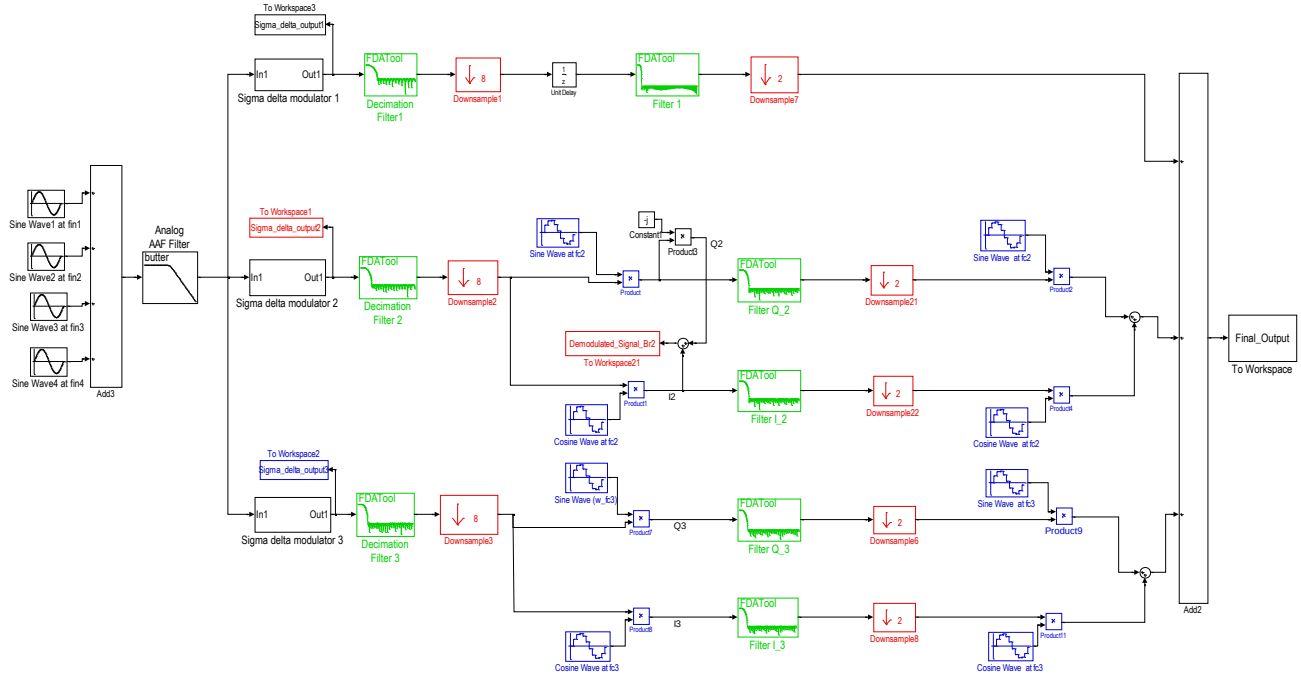


Fig. 5. Proposed FBD-based ADC architecture model with demodulation-based digital reconstruction.

For the first branch, only decimation and filtering operations are needed for the digital reconstruction since it operates at low-pass frequencies as shown in Fig. 4. The global decimation factor is fixed at 16 which is an integer number that permits digitizing UMTS signals at a Nyquist frequency equal to 4.5 MHz. This Nyquist band is comprised between the channel bandwidth, Ch_{BW}, and spacing between UMTS channels, Ch_{sp}, that are specified by design specifications for UMTS standard [7]. The decimation operation is always preceded by a decimation filter that serves as an anti-aliasing filter at the down-sampling frequency. To reduce the complexity of such a decimation filter with a high decimation factor, the authors opt to two-stage decimation. The first stage ensures decimation by a factor of 8 and the second by 2.

For the second and third parallel branches that operate in band-pass frequencies, the digital reconstruction is composed of the operations of demodulation, decimation, filtering and remodulation as explained by Fig. 4. The complex demodulation as explained before consists in multiplying the ΣΔ modulator output by a discrete exponential signal at the branch central frequency as given by (1). In the Matlab/Simulink model, the authors replace the complex demodulation and remodulation by in phase (I) and quadrature (Q) paths to assure better conditions for implementation. The demodulation should then be followed by filtering of the unwanted frequencies which are due to the demodulation operation. This filter presents high complexity since the unwanted frequencies are at low values and the filter operates at the oversampling frequency of the ΣΔ modulator. To deal with this problem, the authors opt to place the demodulation operation after the first decimation stage with a factor of 8. This solution permits to reduce operating frequency of the filter following the demodulation. Moreover, it allows combining this filter with the second stage decimation filter and the low-pass filter that selects the branch bandwidth signals and rejects the quantization noise at the adjacent branches bandwidths. The first decimation stage placed at the ΣΔ modulator output is composed of an operation of decimation by a factor of 8 preceded by a LP FIR decimation filter. The orders of this filter at the first, second and third branches are chosen to be 29^{th}, 39^{th} and 56^{th}, respectively. Then, the LP FIR filters of branch's bandwidth selection are chosen of order 82^{th}.

The frequency response of these filters after remodulation of the second and third ones is presented by Fig.6. The filters responses are overlapping. Their intersection is at level around -6dB and at the frequencies limits between adjacent branches as shown in Fig.6.

The module of the frequency response of the sum of the different filters is presented by Fig.7. The magnitude response presents ripples and attenuations at the frequencies limits that do not exceed 2 dB as shown in Fig.7 (b). Thus, Expected performances of the reconstruction system are not affected.

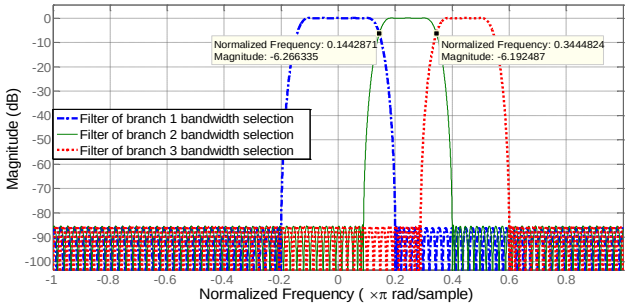
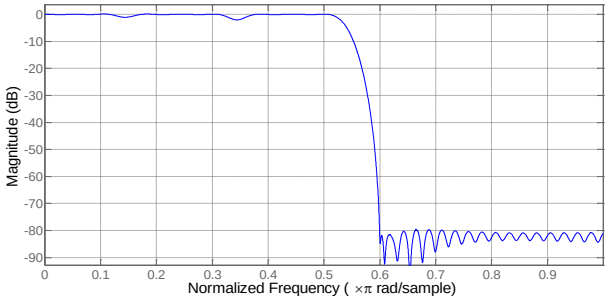
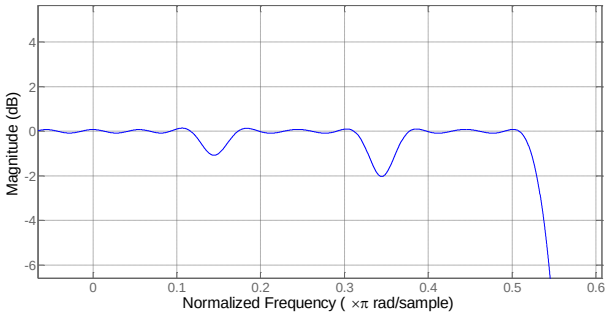


Fig. 6. Magnitude of the LP filters of 82^{th} order after remodulation.



(a)



(b)

Fig. 7. (a) Magnitude of the sum of LP filters of 82^{th} order after remodulation, (b) zoom to show ripples.

After decimation and filtering operations, the I and Q paths are remodulated to return the sub-band signal around its original frequency. Finally, the sub-band output signals are recombined to obtain the reconstructed UMTS signal.

Some simulation results are presented in section IV.

IV. SIMULATION RESULTS

Simulation results are realized by applying a multi-tone signal composed of four sine-wave signals to the FBD model shown in Fig. 5. The first and last sine-wave frequencies are placed in the bandwidths [0, 600 kHz] and [1500 kHz, 2500 kHz] of the branches 1 and 3, respectively. The selected values are 300 kHz and 1900 kHz. The first branch central frequency, f_{c_1}, and the third

branch central frequency, f_{c_3}, are equal to 300 kHz and 2000 kHz, respectively. The two other sine waves are at frequencies in the 2nd branch bandwidth. They are situated on both sides of the 2nd branch central frequency, f_{c_2} which is equal to 1100 kHz, and their values are 700 kHz and 1300 kHz.

In fact, the authors test the UMTS FBD second branch with a two-tone signal to verify the proper functioning of the I/Q demodulation and remodulation. The sine-wave normalized amplitudes are set at 0.5 for the first and last sine waves and at 0.25 for the sine-waves of the 2nd branch where the normalized amplitude is the input amplitude out of the power supply voltage [5].

The zoom of the spectrum over [-4.5, 4.5 MHz] of the second branch sigma delta modulator output, Sigma_delta_output2, is drawn in Fig. 8. It is shown that the sine-wave signals are at the frequencies 700 kHz and 1300 kHz as chosen in the test conditions. To present I/Q demodulated signal of the 2nd branch as in Fig. 8, the authors need to recombine a complex demodulated signal, Demodulated_Signal_Br2 as defined in Fig. 5. The sampling frequency after decimation is equal to 9 MHz and the spectrum is in [-4.5 MHz, 4.5 MHz]. The obtained sine-wave signals are at the frequencies 200 kHz and -400 kHz which are the frequencies of the needed demodulated sine-wave signals. However, the sine-wave signals at the frequencies -1800 kHz and -2400 kHz are unwanted signals that are filtered thanks to the filters, FilterI_2 and FilterQ_2, following the demodulation stage.

The recombined final output signal spectrum in [-2.25 MHz, 2.25 MHz] is presented in Fig. 9. It is shown that the remodulated signals are correctly at the values ±300 kHz, ±700 kHz, ±1300 kHz and ±1900 kHz which corresponds to chosen values of the test conditions of the simulation results. Indeed, the signal-to-noise ratio (SNR) computed using Simulink/Matlab is equal to 75.06 dB which responds to the required dynamic range for UMTS signal which is equal to 73.8 dB.

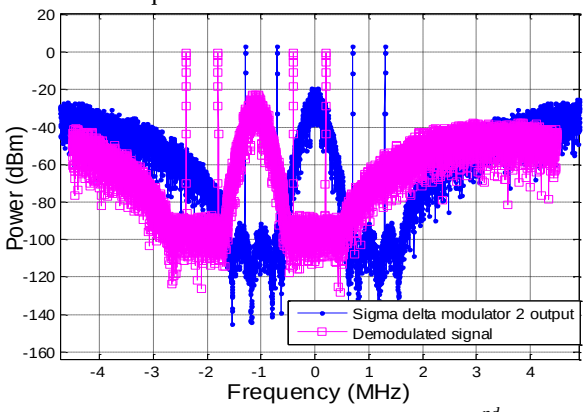


Fig. 8. Demodulated signal spectrum at the 2nd branch.

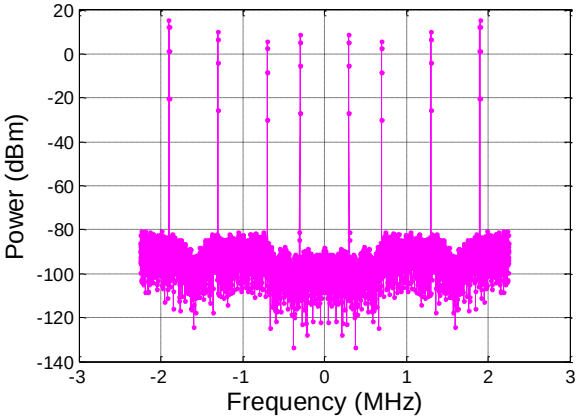


Fig. 9. Recombined output signal spectrum.

V. CONCLUSION

In this paper, the design of a digital reconstruction stage for a FBD ΣΔ-based ADC architecture dedicated to multistandard radio receiver is proposed. The proposed digital reconstruction stage is based on demodulation that brings the ΣΔ modulators outputs to baseband before proceeding to decimation and LP filtering operation. The parallel signals are then remodulated and combined to form a final output signal. The whole FBD ΣΔ-based ADC architecture model with the designed digital reconstruction stage is implemented and tested for the UMTS use case using Matlab/Simulink.

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