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A real-time compensation method for MV voltage transducer for power quality analysis

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Abstract- The growing need of power quality analysis in medium voltage grids leads to the employment of transducers with wider and wider bandwidth. This requirement is in contrast with the need of adopting a low cost hardware for capillary monitoring. Therefore, in this paper a technique for the extension of the frequency bandwidth of MV voltage dividers is presented. The performance of the compensated dividers is comparable with that of dividers of better accuracy class, but the cost is kept low.

I. Introduction

The growing need of power quality analysis in medium voltage grids, required by the increasing diffusion of distributed generation sources, has led to the employment of transducers and measurement techniques able to convert and acquire voltage signals with improved accuracy. Many applications require the use of transducers with wide frequency bandwidth ([1]-[5]), like power quality measurements ([6]-[10]), measurements on photovoltaic plants ([11], [12]), energy and power meter calibration ([13]-[16]). For this purpose, voltage dividers which show higher frequency bandwidth and better linearity than conventional voltage transformers are becoming the most used transducers in power quality assessments. However, disadvantages like a higher dependency on the divider transfer function from environmental conditions (temperature, proximity effects) are introduced. The proximity effects can be reduced by shielding the device([17]); this produces an increase of the stray capacitive coupling among the elements whose strength varies with the insulation medium. Many dividers, for economic and safety reasons, make use of resin as an insulating medium whose electric characteristics can strongly depend on temperature, voltage and frequency with non linear laws ([18], [19]). With the aim of improving the performance of these dividers, so allowing their applications to grids with severe electrical and environmental conditions like the railway feed systems and on board MV circuits, a real time compensation method is proposed. It is based on the identification of a digital filter, with frequency response equal to the inverse of the divider, which is executed on a FPGA, equipped with A/D and D/A converters. As a first application, the transfer function for the frequency compensation of two MV dividers is identified.

II. Divider features

The compensation technique is applied to two dividers with different frequency behaviour. One is a pure resistive divider (RD) and the other is a resistive-capacitive divider (RCD). The highest voltage for equipment (U_m) is 24 kV for both. The resistive divider has a rated scale factor K_{NOM} of 10000 and a 30 MΩ high voltage arm. The RCD, whose K_{NOM} is 1000, is made, for the MV arm, of a series of 20 cells. Each cell consists of a 10 MΩ non-inductive thin film resistor ([18], [19]) and a 1.5 nF ceramic class 1 capacitor, parallel connected. For the low voltage arm an equivalent resistance of 155 kΩ and 116.4 nF ceramic capacitors are used. The MV cells are disposed in four layers, each one made of five cells, which are series connected following an opposite path to minimize the stray inductances. A two sections cylindrical shield allows the control of the capacitive coupling due to the surrounding structures (Figure 1). Both the dividers are resin insulated, with a consequent downgrade of their performances. The two divider transfer functions show dynamic behaviours strongly different (Figures 2 and 3). The scale factor and phase error of RD (Figure 2) have an overall variation of 30 dB and about 1.2 rad respectively over 4 decades, while the RCD (Figure 3) shows 12 % and 100 mrad of variation over the same frequency range. The so different frequency behaviour of the two dividers represents an interesting test bench for the compensation technique. In fact the identification of the parameters of the compensation transfer function requires a growing effort from RD to RCD.

III. Divider characterization

The vectorial frequency response of a voltage divider with a scale factor higher than 1000 requires characterised measurement system able to compare voltage phasors whose amplitude differs of three orders of magnitude. This can be performed by means of digitisers coupled with an attenuator probe or a reference divider, with high scale

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factor and frequency response up to at least 1 MHz. As an alternative, to perform the frequency sweep at low voltage (e.g. hundreds of volt), without making use of a reference voltage transducer, two Agilent 3458 multimeters (DMMs) are employed as digitizers. They have full scales from 100 mV to 1000 V and frequency bandwidth up to 12 MHz, depending on the selected digitizing technique. The synchronization between the two multimeters is provided by an external trigger supplied by a waveform generator. Before introducing the measurement circuit, some aspects on DMM digitizing methods are discussed in the following.

A. Multimeter digitizing methods

The multimeters provides three digitizing methods: DCV, Direct Samplig and Subsampling. Two of them, DCV and sub-sampling, are implemented for the divider frequency characterisation. By DCV technique, the signal is acquired just in DC mode, and the sample is obtained by integration of the input signal, over a specified integration time interval, that can be varied from 500 ns up to 1 s. The technique offers speed and resolution tradeoffs from 18 bits (5 l/2 digits) at 6 kSa/s to 16 bits (4 l/2 digits) at 100 kSa/s, as well a high input impedance However, the maximum sample rate of 100 kSa/s associated with a bandwidth limited to 30 kHz for 100 V and 1000 V full scale makes this digitizing technique not adequate to perform the frequency analysis up to 100 kHz, but it ensures a high magnitude and phase accuracy up to tens of hertz. The sub-sampling technique employs a track and hold (T&H) circuit which performs the signal integration over a very small interval (2 ns) and holds the integrated sample during the slower A/D conversion.

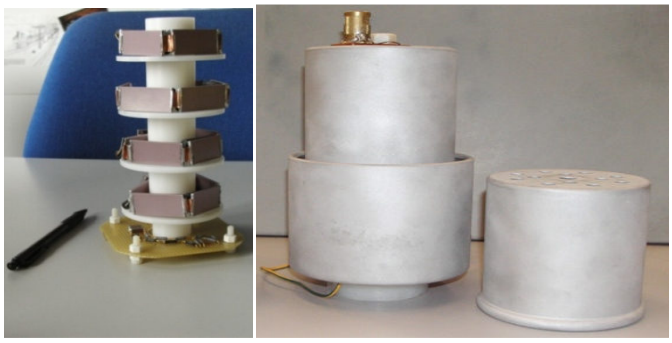
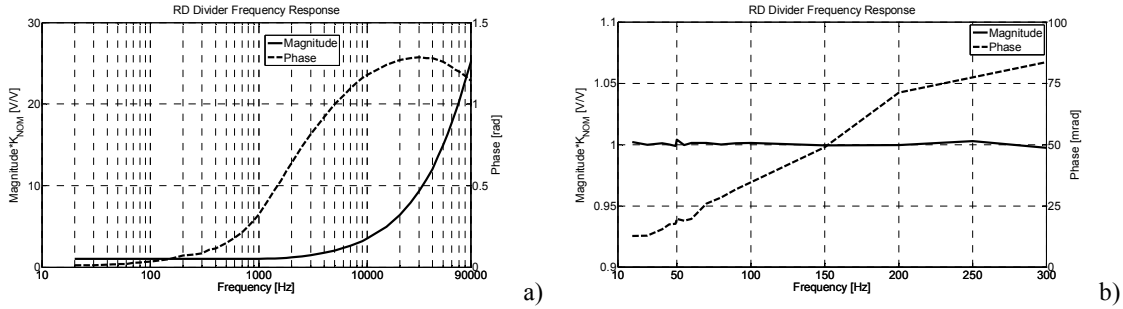
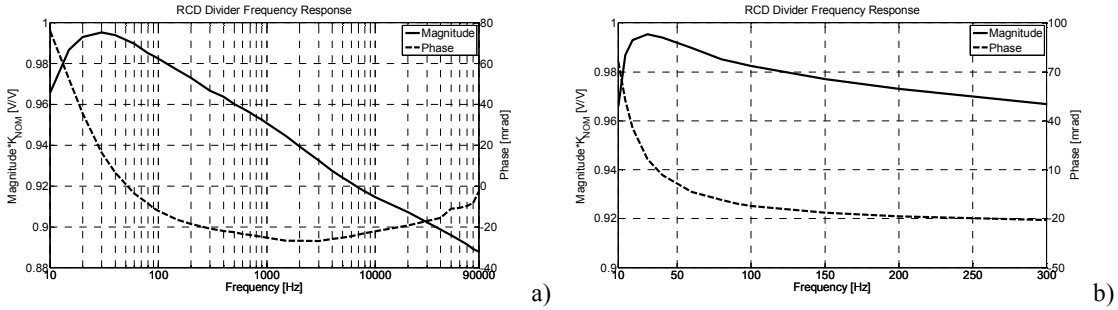


Figure 1. Resistive-capacitive shielded divider during the assembly step



a) b)

Figure 2. frequency behaviour of RD divider between 10 Hz and 200 kHz a) and zoom between 0 Hz and 300 Hz b)



a) b)

Figure 3. frequency behaviour of RCD divider between 20 Hz and 200 kHz a) and zoom between 0 Hz and 300 Hz b)

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The required A/D time conversion limits the actual sample frequency to 50 kSa/s, but thanks to the sub-sampling algorithm the sampling frequency reach 100 MHz. The bandwidth at 100 V peak full scale is limited to $1 \cdot 10^8$ [V·Hz] it means that at 100 V the bandwidth drops to 1 MHz. Table I summarizes the frequency bandwidth, the input impedance and the best accuracy for the employed scales and digitizing methods.

B. Measurement set-up

The measurement set-ups for the Subsampling and DCV digitising methods are shown in Fig. 4a and 4b respectively. In both cases the trigger signal is given by a waveform generator. For the DCV mode, a 5 V square wave signal triggers the simultaneous acquisitions of each sample by the two multimeters and the applied voltage is given by a power amplifier (DC - 500 kHz, 120 V) supplied by a calibrator.. When the subsampling technique is used, the output of the waveform generator supply the power amplifier and the available SYNC output triggers the two multimeter acquisition sequence. Since with this approach the multimeter time base is used, errors can be introduced because of slightly differences in the two timebases. Because of its better accuracy at low frequency (within 400 μrad up to some hundreds of hertz for the phase, when introducing corrections for the use of scales with different bandwidth), the DCV method is employed from 10 Hz to 60 Hz. As to the subsampling technique, a time delay of 25ns, due to the different latency on the trigger for the two DMMs, becomes relevant in terms of angle for frequecies higher than 10 kHz. This systematic error is corrected but the overall accuracy degrades. Moreover,approaching 100 kHz the accuracy furhter decreases because of the bandwidth which is limited to 1 MHz for the 1000 V scale. The measurement uncertainty is conservatively estimated to be 500 ppm and 5 mrad at 100 kHz for the scale factor and phase errors. The magnitude a phase and DC component of each voltage signal is estimated by applying a fitting algorithm to the acquired samples over 10 periods.

Since the waveform generator and the calibrator provides signals with very low distortions, no higher harmonics besides the DC and the fundamental one have to be inserted in the fitting procedure, which provides accurate estimation of the amplitude and phase within tens of ppm and microradians respectively.

III. Compensation technique

Since a divider can be considered as a linear system, its frequency response can be expressed by (2), where X and Y are the spectra of the signals, both before and after the transduction. R and φ are systematic modification introduced by the transduction in amplitude and in phase, respectively, on spectral components of input signal.

Table I – Multimeter specifications

	Peak full scale	bandwidth	Input impedance	Best Accuracy
DCV	100 mV	80 kHz	$>10^{10}$ Ω	0.00005 – 0.01%
	1 V	150 kHz	$>10^{10}$ Ω	
	100 V	30 kHz	>10 MΩ	
	1000 V	30 kHz	>10 MΩ	
Sub-Samplig	100 mV	12 MHz	1 MΩ 144 pF	0.02 %
	1 V	12 MHz		
	100 V	12 MHz (1 MHz at 100 V		

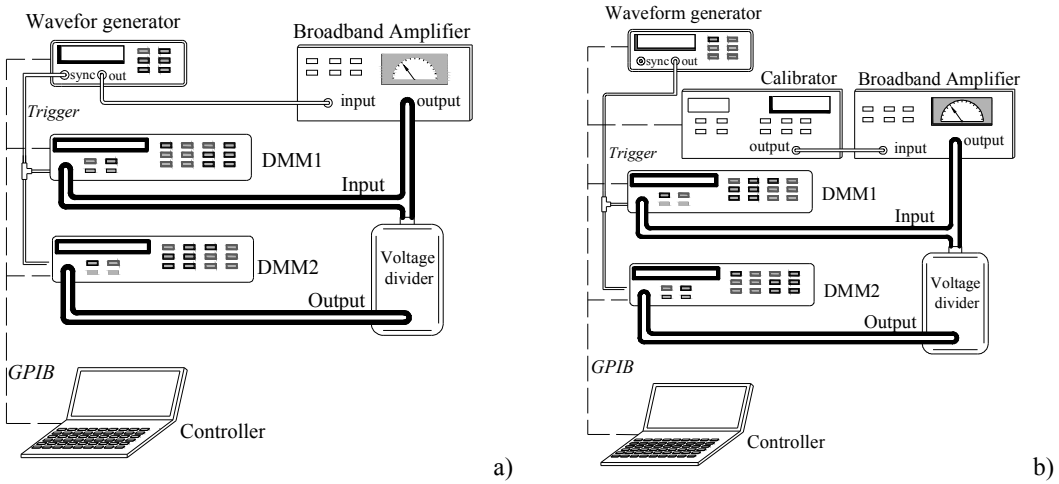

Figure 4. Measurement set-up for sub-sampling digitizing method a) and for DCV method b)

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Once the divider has been metrologically characterized and its frequency response found over a certain frequency range, cascading a device with a frequency response equal to Divider inverse one, systematic deviations are compensated over all the considered frequency range. For this purpose ([20]-[23]), a filter can be adopted, whose frequency response, $H_d(f)$, should be exactly given by (2), for any frequency, f, in the range of interest. The analog implementation of transfer function (2) is not easily practicable and it can lead to acceptable results only if applied to a very limited frequency range. Better results can be obtained with a digital filtering. Obviously, for a real-time compensation, a digital processor has to implement such digital filtering. For the case at hand a FPGA has been chosen: it implements an IIR filter which is generally modeled by a transfer function in z-domain that can be written as (3).

$$Y(f) = \frac{1}{R(f)e^{-j\varphi(f)}}X(f) \quad (2), \; H_d(f) = R(f)e^{-j\varphi(f)} = \frac{X(f)}{Y(f)} \quad (3), \; H(z) = \frac{b_0 + b_1 z^{-1} + \cdots + b_m z^{-m}}{1 + a_1 z^{-1} + \cdots + a_n z^{-n}} \quad (4)$$

With this approach, filter design requires the choice of the best values for the $n+m+1$ parameters $a_1, \ldots, a_n$ and $b_0, b_1, \ldots, b_m$ so that the transfer function of the filter approximates a desired frequency characteristic.

The problem of choosing the best coefficients can be formulated, from a mathematical point of view, as an inverse problem [4] and solved by adopting optimization techniques. An objective function, describing the difference among desired frequency response and obtained values has to be defined and minimized by an optimization algorithm. As it is said in [20], if filter transfer function, $H(z)$, is factorized in second order sections (SOS), frequency response is less sensitive to changes in coefficient values. This factorization can be expressed as (5). In addition, for objective function, the expression (6) is used.

$$H(z) = K\prod_{k=1}^{N}\frac{1 + b_{1,k}z^{-1} + b_{2,k}z^{-2}}{1 + a_{1,k}z^{-1} + a_{2,k}z^{-2}} \quad (5) \qquad F(P) = \frac{1}{2}\sum_{i=1}^{M} W \cdot |\log_{10} H(f_i, P) - \log_{10} H_d(f_i)|^2 \cdot [\log_{10} f_{i+1} - \log_{10} f_{i-1}] \quad (6)$$

In (6), P is the vector of the $4N+1$ variables of (5), M is the number of the frequency points involved in the identification procedure and W is the vector of the weights. The cost function (5) weighs the ratio, rather than the difference, between the model frequency response and the frequency response data at each frequency. In addition, a logarithmic spaced frequency interval has been used. Practically it is like including Bode's concept in the cost function, in fact, it weighs the difference between Bode diagrams of the model frequency response and the frequency response data. It is important to note that this is the real problem as what is really requested to minimize the difference between the Bode diagrams of model and data. In order to numerically study the (4), a hybrid scheme based on the combination of a stochastic and deterministic approach has been adopted and it has been applied to the problem of compensation of the two divider frequency responses.

The procedure has been performed varying the number of SOSs; every execution is repeated three times. Sampling frequency has been chosen equal to 200 kHz. Figure 5 and Figure 6 show the improvement obtained by compensation, in ratio error and phase displacement, for the two dividers. For RD divider, the improvements are about 161.4 and 1.4 respectively for ratio error and phase displacement. For RCD divider, the improvements are about 31.4 and 22.8 respectively for ratio error and phase displacement. Table II and Table III show the coefficients of the best compensating filters for, respectively, the RD and the RCD dividers.

Figure 7 shows the RD divider inverse's and its compensating filter frequency responses, while Figure 8 shows ratio error and phase displacement of compensated RD divider. Figure 9 shows the RCD divider inverse's and its compensating filter frequency responses, while Figure 10 shows ratio error and phase displacement of compensated RCD divider.

IV. Conclusions

The growing need of power quality analysis in medium voltage grids leads to the employment of transducers with wider and wider bandwidth. This requirement is in contrast with the need of adopting a low cost hardware for capillary monitoring. Therefore, in this paper a technique for the extension of the frequency bandwidth of MV voltage dividers is presented. The adoption of the compensation technique allows to reach improvement in dividers performance up to a factor 160. In this way the performance of the compensated dividers is comparable with that of dividers of better accuracy class, but the cost is kept low.

Table II. Coefficients of the best compensating filter for RD divider

b_0	b_1	b_2	b_3	b_4	b_5	b_6
626.80	749.95	-415.10	-230.50	35.625	-4.3313	-6.7867
-	a_1	a_2	a_3	a_4	a_5	a_6
-	-0.46864	-0.96937	0.50844	0.0063371	-0.0026524	0.00017674

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Table III. Coefficients of the best compensating filter for RCD divider

b_0	b_1	b_2	b_3	b_4
1111.8	-615.8	-1090.4	626.8	-9.1506
-	a_1	a_2	a_3	a_4
-	-0.53772	-0.98070	0.54920	-0.0078201

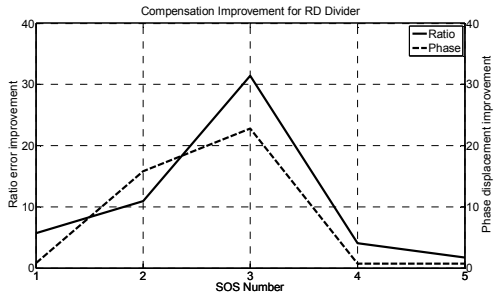

Figure 5. Compensation improvement for RD Divider

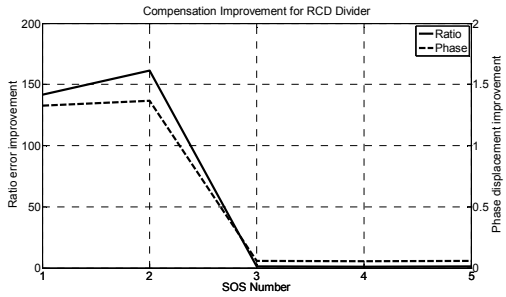

Figure 6. Compensation improvement for RCD Divider

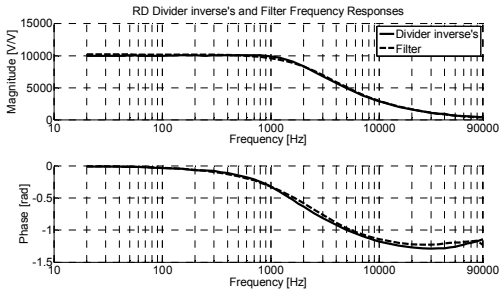

Figure 7. RD divider inverse's and its compensating filter frequency responses

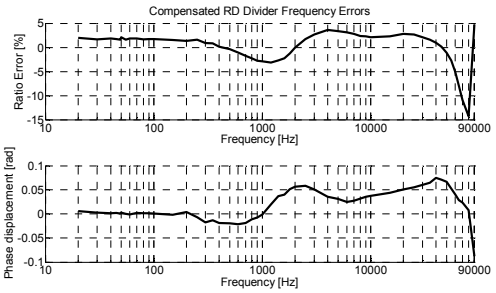

Figure 8. Ratio error and phase displacement of compensated RD divider

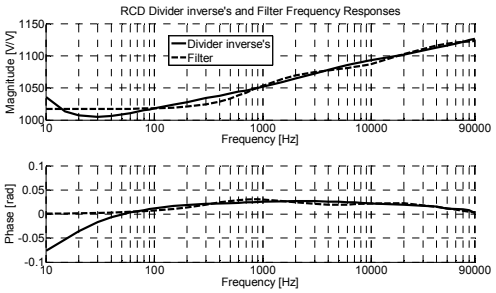

Figure 9. RCD divider inverse's and its compensating filter frequency responses

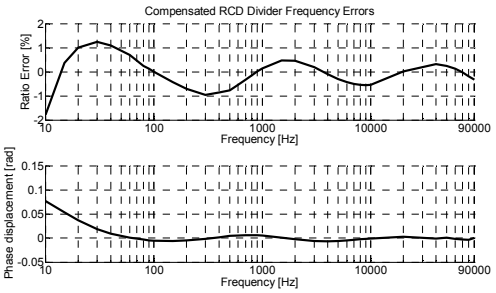

Figure 10. Ratio error and phase displacement of compensated RCD divider

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