Architecture of the Multi-Tap-Delay-Line Time-Interval Measurement Module Implemented in FPGA Device

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ABSTRACT

This paper describes architecture of the Multi-Tap-Delay-Line (MTDL) time-interval measurement module of high resolution implemented in single FPGA device. A new architecture of the measurement module enables to collect of sixteen time-stamps during single measuring cycle. It means that measured time-interval can be precisely interpolated from collection of the sixteen time-stamps after each measuring cycle. Such architecture of the measurement module leads straight to increase of resolution, to limit total duration time of the measurements and to decrease of duty cycle of the measurement instrument.

**Keywords:** time-interval measurement, tapped delay lines

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1. Introduction

High resolution TIMS are widely applied in many system. For example they can be applied in quantum cryptography experiments, in characterization of the clock phase fluctuations, in life-time measurements of the excited atomic states, in ultrasonic flow-meters or monitoring systems of time-of-flight mass spectrometers [1-8]. Of course, it should be noticed, that system implemented in FPGA devices is not energy-efficient. Limiting the total number of time-interval measurements and increasing, in the same time the system resolution, effective duty cycle and the total power consumption could be decreased [9].

The measurement system presented in this paper enables not only for increasing the system resolution but also for significantly decreasing uncertainty of the single time-interval measurement.

1. Architecture of the TIMS

TIMS as a virtual instrument consists of hardware unit, flexible software and a computer.



Figure 1. The block diagram of TIMS.

The block diagram of the new TIMS architecture is shown in Fig.1. The system is implemented in Xilinx Virtex 4 FPGA structure and uses chip-outside-located 64 MB DDR of RAM for data collection.

The main unit of system is 32 bit soft processor – Microblaze. Other parts of the system are implemented as microprocessor peripherals. ISE and EDK programming tools have been used for implementation of the virtual microprocessor (MicroBlaze), that has been programmed in C language and its peripherals.

The implemented system consists of the group of sixteen two-hundred-element multi-tap delay lines with coupled registers, sixteen code converters, four clock cycles counters, blocks of inside memory (BRAM), interface and control unit. Carry chain of CLB’s (Configurable Logical Block) is used to tapped delay lines and registers implementation [Fig. 2]. It is possible to change of the elements placement and connection to change of the line delay. Using this method, the characteristics of delay-line can be shaped.

Data transferred to personal computer is worked out by the Python-script-language that allows, in a simple way, to obtain very efficient, multiprocessor programming environment. These scripts also generate corrected VHDL and UCF (User's Constraints File) source files, so the process of designing measuring module is fully automated. Mainly the location of TDLs and the order of their output is corrected. The system can be calibrated without the need of reprogramming. The calibration module can be removed (turned off) after calibration is done, so the power consumption can be decreased, that extends battery life-time.

First the tap's must be sorted, because time of clock (clk) net is not monotonic [Fig.3]. The values read from the FPGA editor, do not contain information about the fluctuations of the delays in FPGA structure. For this reason, system can read all TDL registers in raw mode, bypassing code converter and storing it in BRAM. It is not possible to read all the sixteen TDL states at the same time (there is not enough BRAMs for this operation implementation on the chip, which was used). There is 16-to-1 multiplexer to switch between TDL's registers. Another signal multiplexer can switch either to the divided by N built-in clock (100 MHz) or external pulse signal. The raw waveform of recorded system clock is triggered by the divided by N built-in clock and then is stored in BRAM. Data from BRAM is sent to computer.

Table 1. The exemplary section of waveform before sorting a) and after sorting b) the tap 97, 98 and 100 is accordingly shifted into place and now their taps numbers are respectively 100, 97, 98

a)

b)

Calibration program on PC computer is seeking anomalies (bubbles) in waveform [Tab.1]. The anomalies can be single, double and so on. Reordered zeros or ones usually appear at the beginnings and the endings of sequences obtained for the same values. The program uses a special correlation procedure to obtain the right order of all taps implemented in the FPGA structure. The next procedure generates VHDL code of the sorted TDL. This procedure is being repeated for every TDL. After compilation the corrected TDLs are implemented in FPGA.

Quadruple of the clock cycles counter ensures sufficient set-up time during incrementation and the possibility of asynchronous read-out of data from one of the counter. The most proper counter is being chosen on the basis of the information obtained from particular TDL. These data are used for computing all sixteen time-stamps from all TDL.

Each measured time stamp consists of main part, which is taken from one of the clock cycles counters and residual part, which is taken from one of the TDL-registers and then compressed to binary-natural-code. The theoretical precision of TDL is 25 ps.



Figure 2. Two taps of TDL made of carry-chain with registers before tuning.

There is a great difficulty to implement the code converter, which converts from thermometric code to binary-natural-code. The main reason to use code converter is limitation of data memory size and speed of data transfer. Single time-interval measurement can generate more than four hundred bytes of data. This value is similar in size to the capacity of the one BRAM inside chip. The code converter reduces about hundred-folds data for storage.



Figure 3. Example of “clk” net delay in FPGA device for 128 slices – read from the FPGA editor.

Requirements for a code converter are compromise of speed and occupancy of small space of FPGA chip. To achieve it many converters 16-to-4 bits in parallel mode were implemented. Finally, the chosen code-converter requires only two BRAM for one TDL in comparison to more than six without code converter.

The DDR of capacity 64 MB RAM is used for data acquisition. In case when there is more than five hundred time stamps in one series and the intensity of measurement time-interval is too fast (more that 100 k samples per second) data is sent to the PC indirectly through the DDR, that allows to obtain about 4 thousand times more space for measurements.

1. Principle of Time-interval measurement

 The main task of the measuring system is registration and collection of time-stamps. The time-stamp is a combination of integer number of standard clock cycles and the TDL-register two-bits index that have 1 to 0 transition registered. The measured time-interval Δtm is calculated by the difference of two time-stamps.



Figure 4. The idea of multiple TDLs measurement.

Precision of TIMS in practice depends on the precision of interpolators, that measure residual time intervals and accumulated jitter of standard clock [9]. If a multi-tap delay lines are used in the design of interpolator then value of the single segment delay τ and its standard deviation determines precision of time-interval (Δtm) measurement. If interpolator consists of n delay lines of relatively high resolution, then during the single measuring cycle it is possible to obtain n different results of time-interval Δtm [10, 11]. Such solution leads straight to increasing of precision of time-interval measurement and reduces number of measurement cycles. This method significantly reduces the power consumption for battery-powered systems, because the number of measuring cycles is generally significantly decreased. Knowing delay lines characteristics such DNL (Differential Nonlinearity) and INL (Integral Nonlinearity) and using quantization-and-nonlinearity-minimization (QNM) method, it is possible to obtain two-sample-difference histogram, increases system resolution and decreases uncertainty of time-interval measurement [12].

In the presented system with 16 TDLs which consists of 200 taps (for each TDL), expected accuracy should be better than 15 ps for single-shot measurement.

1. Experimental Results



Figure 5. The experimental measurement system.

A series of time-interval measurements was performed to verify the measurement system. For the test, a single section of coaxial cable was used as a delay element as it is shown in Fig.5.



Figure 6. Time-stamp histogram obtained for start pulse.



Figure 7. Time-stamp histogram obtained for stop pulse.

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Figure 8. Time-interval histogram

Figures 6 and 7 show time-stamp histograms obtained for start and stop pulses. One should notice that the surfaces of both diagrams are equal to the number of TDLs. Figure 8 shows time-interval histogram obtained as a difference between start and stop measurements. It is worth of being noticed that the uncertainty of time-interval does not increased significantly in comparison to source time-stamp uncertainties.

1. CONCLUSIONS

Designed time-interval measuring system allowed obtaining higher precision of measurements thanks to measurements realized simultaneously by 16 TDLs at the same time. Measurements for every hit are realized parallelly, so the measuring time is not increased, as well as the energy consumption is limited, because the measuring module can go into stand-by mode periodically for a longer time.

Obtained time-interval histograms are characterized by low uncertainty in comparison to time-stamps uncertainties even though TDLs characteristics are very nonlinear, because the QNM method takes into account the characteristics of TDLs.

The process of designing the measuring module has been fully automated that has been especially useful for TDLs implementation. The TDLs output wires are automatically rotated to obtain proper thermometric codes that allowed the implementation of TDLs with the precision that is equal to one carry element delay.

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