Dear Editor,

Please find our extended and substantially changed paper for the Special Issue attached to this submission. Please also find below the summary of the differences between the conference paper and the special issue paper;

Our paper “Novel Time-Interleaved Variable Centre-Frequency, Single-Bit A/D and D/A Sigma-Delta Modulator Topologies” submitted to XIX IMEKO TC-4 Symposium conference has been technically extended with the authors’ recent studies on the subject.

In the Special issue paper, “Design and Implementation of Novel FPGA Based Time-Interleaved Variable Centre-Frequency Digital Σ−Δ Modulators”, the following extended work is presented:

* The designed digital single-path and time-interleaved sigma-delta modulators in XIX IMEKO TC-4 Symposium paper are implemented in VHDL and synthesized on the Xilinx® SpartanTM-3 Development Kit to validate the design methodology presented.
	+ The experimental results of the implemented circuits are compared with the behavioral-level topologies in terms of tonality and signal-to-noise ratio.
	+ The designed discrete-time analog sigma-delta modulators in XIX IMEKO TC-4 Symposium paper are not included in the scope of this modified paper.
	+ The hardware sources allocated for the designed modulators are summarized.
* The mathematical model of the quantization tones of these sigma-delta modulators under sinusoidal input excitation is discussed covering the digital time-interleaved sigma-delta modulators.

Kind Regards;

Isil Kalafat Kizilkaya, Mohammed Al-Janabi, Izzet Kale