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A cost-efficient reversible logic gates implementation based on measurable quantum-dot cellular automata

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ABSTRACT
In order to improve the density on a chip, the scaling of CMOS-based devices begins to shrink in accordance with Moore's laws. This scale affects the execution of the CMOS device due to specific limitations, such as energy dissipation and component alignment. Quantum-dot cellular automata (QCA) have been replaced to overcome the inadequacies of CMOS technology. Data loss is a major risk in irreversible digital logic computing. As a result, the market for nano-scale digital operations is expanding, reducing heat dissipation. Reversible logic structures are a strong competitor in the creation of efficient digital systems. A reversing logic gate is an important part of reversible circuit design. The QCA design of basic reversible logic gates is discussed in this study. These gates are built using a new QCA design with XOR gates with two and three inputs. QCADesigner tests simulation performance by simulating the specified reversible logic gate layouts. The measurement and optimization of design techniques at all stages is required to reduce power, area, and enhance speed. The work describes experimental and analytic approaches for measuring design metrics of reversible logic gates using QCA, such as ancilla input, garbage output, quantum cost, cell count, and area, while accounting for the effects of energy dissipation and circuit complexity. The parameters of reversible gates with modified structures are measured and then compared with the existing designs. The designed F2G, FRG, FG, RUG and UPPG reversible logic gates using QCA technology shows an improvement of 42 %, 23 %, 50 %, 39 % and 68 % in terms of cell count and 31 %, 20 %, 33 %, 20 % and 72 % in terms of area with respect to the best existing designs. The findings illustrate that the proposed architectures outperform previous designs in terms of complexity, size, and clock latency.

Section: RESEARCH PAPER

Keywords: Majority gate; Quantum dot cellular automata, reversible logic; reversible gates

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1. INTRODUCTION

The building of digital logic circuits using reversible logic gives a zero dissipation of electricity. For irreversible calculations, Landauer [1] established that each logical bit of data loss results in $k_B T \ln(2)$ joules of heat energy. Lent et al. [2] demonstrated that zero-energy dissipation in a digital logic circuit is only possible if the circuit is made up of reversible digital logic gates. The energy systems quantum-dot cellular automata (QCA) circuit dissipation can be significantly lower than $k_B T \ln(2)$ because QCA circuitry is clocked systems that maintain data. This function encourages the use of QCA technology in the construction of reversible digital circuits. Reversibility, on the other hand, reverses bit loss but does not identify bit faults in the circuit. Performance issues can be corrected by using fault-tolerant gates with reversible logic. It becomes simpler and easier to detect and correct defects when the system is made up entirely of fault-tolerant elements. Parity is used to achieve fault tolerance in communications and other systems. Parity-preserving circuitry would thus be the forthcoming architecture principles for the creation of reversible fault-tolerant devices in nanotechnology. Because of its very small size and low power consumption, QCA is recommended for use in nanotechnology research [3]. The basic reversible logic gates make up reversible circuits. These gates produce a one-of-a-kind mapping of input and output pairs, making the set of inputs equal to the total outputs. In [4]-[6], a substantial contribution to the research for the building of basic reversible logic gates was made. These topologies, on the other hand, are less efficient and necessitate greater inverter and majority gate reductions. It aids us in the development of reversible logic gates with fault-tolerant architectures using QCA technology. The basic reversible gates are constructed using upgraded XOR gate designs. Because of the rapid advancement

of QCA technology, a great deal of research has been done in the field of QCA-based reversible logic measurement and technology, with the goal of improving performance metrics in terms of measurement accuracy and complexity, and thus improving the efficiency and precision of circuits. Each reversible logic gate in a reversible logic system architecture measure specific parameter separately. The system then combines all the independents into a comprehensive set of measurement data using updated gate structures. Many parameter values in the existing designs are not measured when the circuits are tested. In individual cases, it might be necessary to make measurements to accurately analyze the behaviour of the reversible logic gates.

1.1. Reversible logic

If each input state yields a different output state, the logic characteristic is reversible. A reversible gate is the kind that realizes reversible functionality. Both outputs and the inputs can have a bijective mapping. As a result, the output and input quantities must be equal in order to prove the reversibility principle. In reversible logic gates, feedback is not acceptable, and fan out is not permitted. The circuits implementation with reversible logic gates are measured with the parameters like primitive gate count, constant input, logic calculation, unwanted output and quantum cost. Based on their features, these gates have indeed been grouped into three types.

• Basic Reversible Logic Gates: all of these gates are necessary parts of a reversible circuit. There have been other reversible gates invented, but NOT as well as BUFFER is the most basic.

• Conservative Reversible Logic Gates: these gates have about the same number of zeros and ones at both inputs and outputs. Consider the case of MCF's Gates.

• Parity-preserving reversible logic gates: these gates have about the same parity (either even or odd) at both their inputs and outputs. Only in terms of mathematics. All of the inputs and outputs of XOR are equal to zero. The conservative gates are retained through parity, while the contrary is not true.

1.2. QCA

In [2], Lent et al. introduced QCA technology, which is utilized to construct all components of a nanoscale QCA circuit. Each QCA cell is made up of four quantum dots, which are nanostructures capable of trapping Electric bills. Because these electrons are repelled by each other due to Coulomb interaction, they seem to be positioned on opposite corners of the square. The alignment of electron pairs defines two potential polarization states, -1.00 and 1.00. The majority gate and the inverter gate are the two most basic QCA gates. Many logic operations that are governed by the clocking operation are commonly executed by the Coulombic interactions of electrons in neighbouring cells.

1.3. Related work

Several studies using QCA to generate reversible logic gates have just been conducted during the previous decade [6]-[11]. QCA architectures using majority gates as the foundation device for numerous reversible gates were shown by researchers in [6]. Because the output lines are not really strongly polarised, these kinds of gates are not considered sufficient. For Fredkin, Feynman, and Toffoli gates, Mohammadi et al. [7] built QCA-based reversible circuits integrating both rotating and normal cells. The architectures shown are dependent on the majority gate's arrangement. However, an effective QCA architecture necessitates a new majority circuit design process, which adds to the complexity. Peres and Feynman's gates based on QCA realisable majority gates were discussed in [8]–[10]. Their topologies are less optimal, necessitating the reduction of both main and inverter gates. The authors of [11] proposed employing majority gates in QCA to create an efficient reversible logic gate arrangement. However, these systems have usual restrictions, such as a higher number of stable input signals. Without employing any wire crossing, the topologies presented by Sing et al. [11] cannot be achieved. The Feynman gate [12] is the well-known "2X2" reversible gate. It can be used to increase fan-out. The famous "3X3" reversible gates are Toffoli, Peres, and Fredkin [13], [14]. Trailokya Nath Sasamal et.al [15] designed reversible gates like FG, FRG, TOFOLLI, Peres gate and F2G in QCA with 26, 68, 59, 88, 53 and 0.03 μm^2, 0.06 μm^2, 0.034 μm^2, 0.097 μm^2, 0.058 μm^2 QCA cell count and area respectively.

The main contributions of the paper are as follows:

1. introduces new optimized layouts for the existing reversible logic gates to reduce the complexity of the circuits.
2. later, the performance of the proposed gates is analyzed and compared with the existing gates using conventional parameters.

2. NOVEL QCA DESIGNS FOR REVERSIBLE GATES

The essential building elements of reversible digital logic are the reversible gates. Such gates produce a one-of-a-kind mapping between the input as well as output sets, allowing for the same combination of inputs as outputs. QCA designs of XOR, F2G (double Feynman gate), FRG (Fredkin gate), FG (Feyman gate), RUG (Reversible universal gate), and UPPG (Universal parity preserving gate) reversible gates are provided in the following section. All of the suggested approaches adhere to the QCA designs rules in aspects of all input cells arriving in a same period clock zone, long QCA wires being subdivided into four clock zones based on the highest cell count in the same zone and the minimum cells in the same zone to avoid increased signal propagation and switching delays, and none of the suggested approaches have crossover choices. The prototypes of several reversible gates have been synthesized and measured using QCA designer tool. An XOR gate is the basic element of the most elementary reversible gates. It has been observed that the endurance of the design of the reversible logic architecture is influenced not only by the complexity as well as by the latency of an XOR gate. Two inverters and three majority gates are required in the classic XOR architecture. The suggested reversible layouts are using integrated architecture with only 12 QCA cell connections for both the 2-input and 3-input XOR gates, as can be seen in Figure 1.

The F2G [16], [18] proposed block diagram and conceptual design are illustrated in Figure 2a. It has three inputs namely A, B, C and three outputs P, Q, R. The F2G concept uses the current XOR gate to produce a design that is optimum for the region. Figure 2b. shows a possible QCA architecture with such a gate. Note that the first input A is carried to P, whereas the realization of two output bits Q and R necessitates the use of two XOR gates having two inputs. The designed F2G gate QCA layout utilizes only two-time clock zones.

Figures 3.a and b illustrate the block diagram and schematic diagram of the hypothesized Fredkin gate. In general terms, the FRG (Fredkin gate) [19]-[24] is called a universal gate in the sense that it may be "trained" to operate as many basic components in almost any reversible digital logic circuit. It has three inputs namely A, B, C and 3 outputs P, Q, R. For deployment, there are

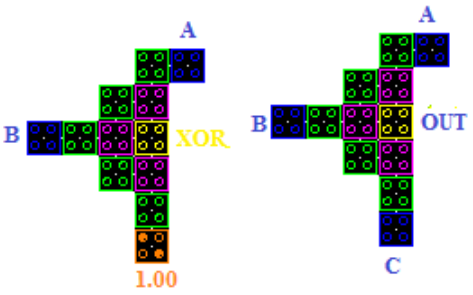
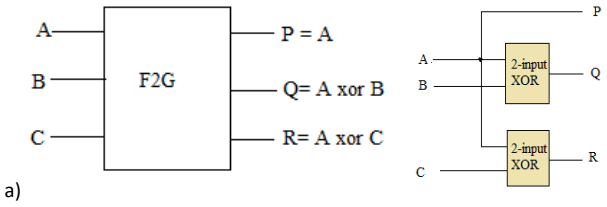
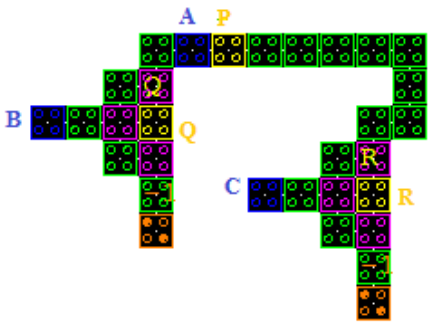


Figure 1. QCA Layout of XOR gate with 2-input and 3-input.



a)



b)

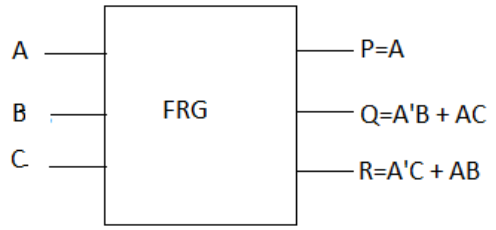
Figure 2. Double Feynman gate (F2G): a) Block diagram and schematic diagram, b) QCA layout.

six primary gates. Figure 3c shows the QCADesigner setup of the built Fredkin gate. The suggested modified FRG gate shows a measurement of only 75 QCA cells. The output signal P is observed to be connected to the input signal A, but the output signals Q and Rare implemented using majority gates. Four-time clock zones are used in the intended FRG gate QCA configuration.

Figure 4 shows the Feynman gate's block diagram and schematic diagram. It uses two inputs namely A, B and two outputs P, Q. Because of its widespread use in quantum computing, the FG (Feynman gate) is sometimes referred to as the controlled NOT or even quantum XOR gate [25]-[28]. The measurement of the designed FG gate is done with a coherence vector simulation engine. Figure 4b depicts the corresponding QCA architecture, which has a single XOR gate with two inputs. It's important to note that output P is related to input A, however output Q necessitates the use of a simpler XOR gate than the present XOR designs. Just two-time clock zones are used in the developed F2G gate QCA [29].

A block and conceptual design for the RUG gate is shown in Figure 5a. It has three inputs and three outputs In Figure 5b, an appropriate QCADesigner interface has been demonstrated for the RUG gate.

There are four primary gates and one XOR gate having two inputs in this circuit. The output P was generated from a three-input majority gate, Q was collected from three majority gates, and R was obtained out of a two-input XOR gate, as shown in



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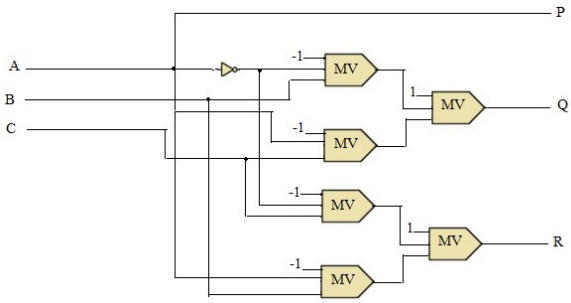

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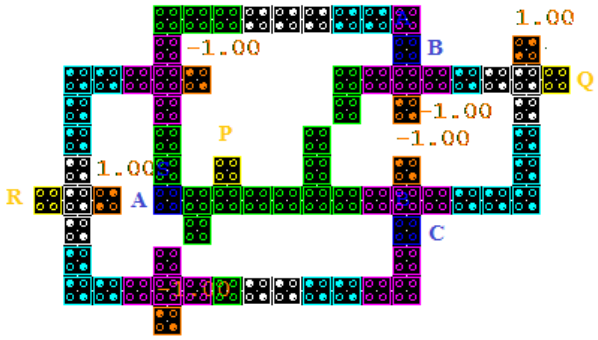
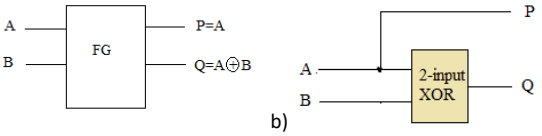


c)

Figure 3. Fredkin gate (FRG): a) Block diagram, b) Schematic diagram, c) QCA layout.

the diagram. Four-time clock zones are used in the intended RUG gate QCA layout.

Figure 6a and Figure 6b illustrate the topology and schematic design of the proposed QCA universal parity preserving gate (UPPG). It has four inputs and four outputs Two majority gates, two XOR gates with two inputs, and one XOR gate with three inputs make up the circuit. The measurement of modified UPPG gate shows a better improvement with the existing designs.



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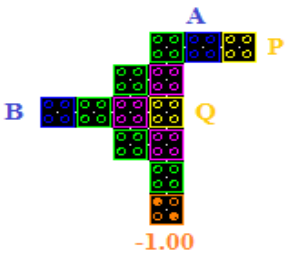

c)

Figure 4. Feynman gate (FG): a) Block diagram, b) schematic diagram, c) QCA layout.

Figure 6c depicts the suggested QCADesigner layout for the UPPG gate. It was discovered that the proposed arrangement has an occupied area of only 0.08 μm². A total of two different time clock zones are used in the UPPG gate QCA configuration.

3. RESULTS AND DISCUSSION

The coherence(accuracy)vector simulator had been used to analyze the layouts using default parameters, and QCADesigner had used QCA configurations of the recommended systems. The cell size, layer separation distance, dot diameter, high clock area, low clock area, clock shift area, clock amplitude factor, relative permittivity, radius of effects, number of tolerances, convergence tolerance, and maximum iterations per sample are 18 nm × 18 nm, 5 nm, $9.800000 \cdot 10^{-22}$ J, $3.80000\ 10^{-22}$ J, 0, 2, 12.9, 85 nm, 4, 0.001, and 100, respectively. The F2G gate simulated waveform is shown in Figure 7. This simulation waveform has demonstrated that the circuit is functional, and consequently output values are created for all input data. For development, 31 cells in an area of around 0.04 μm² are required. Figure 7 shows the results of the Fredkin gate model. This gate is frequently employed as a multiplexer in electronics in a variety of applications. It is made up of 75 QCA cells with 0.08 μm² area widths. The Feynman gate was made using 13 QCA cells with a total area of around 0.02 μm², as shown in Figure 4, and the result of its simulation can be seen in Figure 9. Figure 10 depicts the simulation waveform of the RUG. With a surface area of 0.08 μm², it utilizes 59 QCA cells. The proper operation of the UPPG gate is shown in Figure 11. This gate is made with only 75 QCA cells and a surface area of around 1 μm².

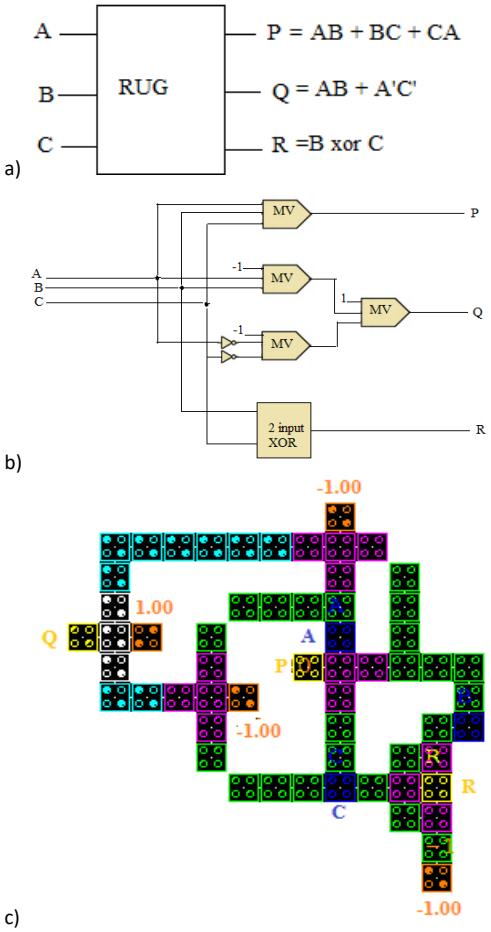

Figure 5. Reversible universal gate (RUG): a) Block diagram, b) Schematic diagram, c) QCA layout.

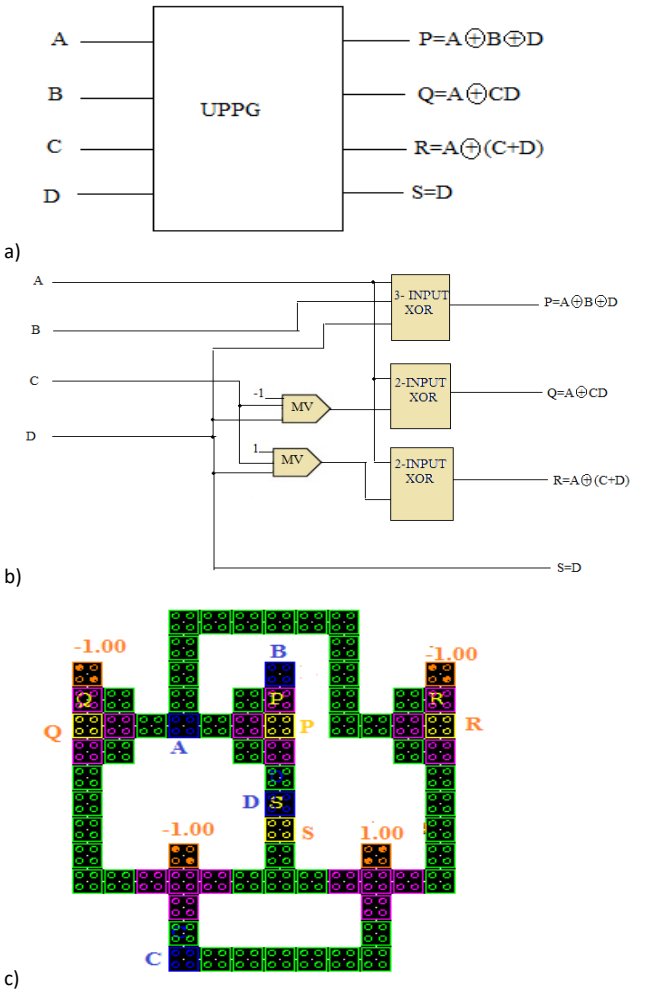

Figure 6. Universal parity preserving gate (UPPG): a) Block diagram, b) Schematic diagram, c) QCA layout.

A study of the characteristics of the recommended reversible gate configurations with the measurement of previous studies is shown in Table 1 to Table 5. Table 1 describes the design F2G reversible gate, which shows an improvement of 42 % and 31 % with respect to QCA cells and area with the best existing design. When we compare the developed F2G to previously described designs, we find that the F2G designed with QCA is the best in terms of the number of QCA cells and the area it supports, as shown in Table 1. Table 2 shows the planned FRG reversible gate, which was built using 75 QCA cells with a measured area of 0.08 μm² and a 0.5 clock cycle delays. It shows that the recommended architecture selected the best of all existing designs. When compared to the optimal design, the suggested FRG gate provides a 23 % and 20 % improvement in cell count and area, respectively. The Fredkin gate presented has been found to be more acceptable for cascade design, and the output metrics are comparable to the same optimal technique. The Fredkin gate seems to have a delay of 0.5 clocks, which is less than that of conventional designs. Table 3 presents the intended FG reversible gate, which was built using 13 QCA cells with a 0.02 μm² area and a 0.5 clock cycle latency. The recommended FG circuit is compared to earlier circuits in Table 3. When compared to the optimal design, the proposed FG gate improves cell count and area by 50 % and 33 %, respectively. The total

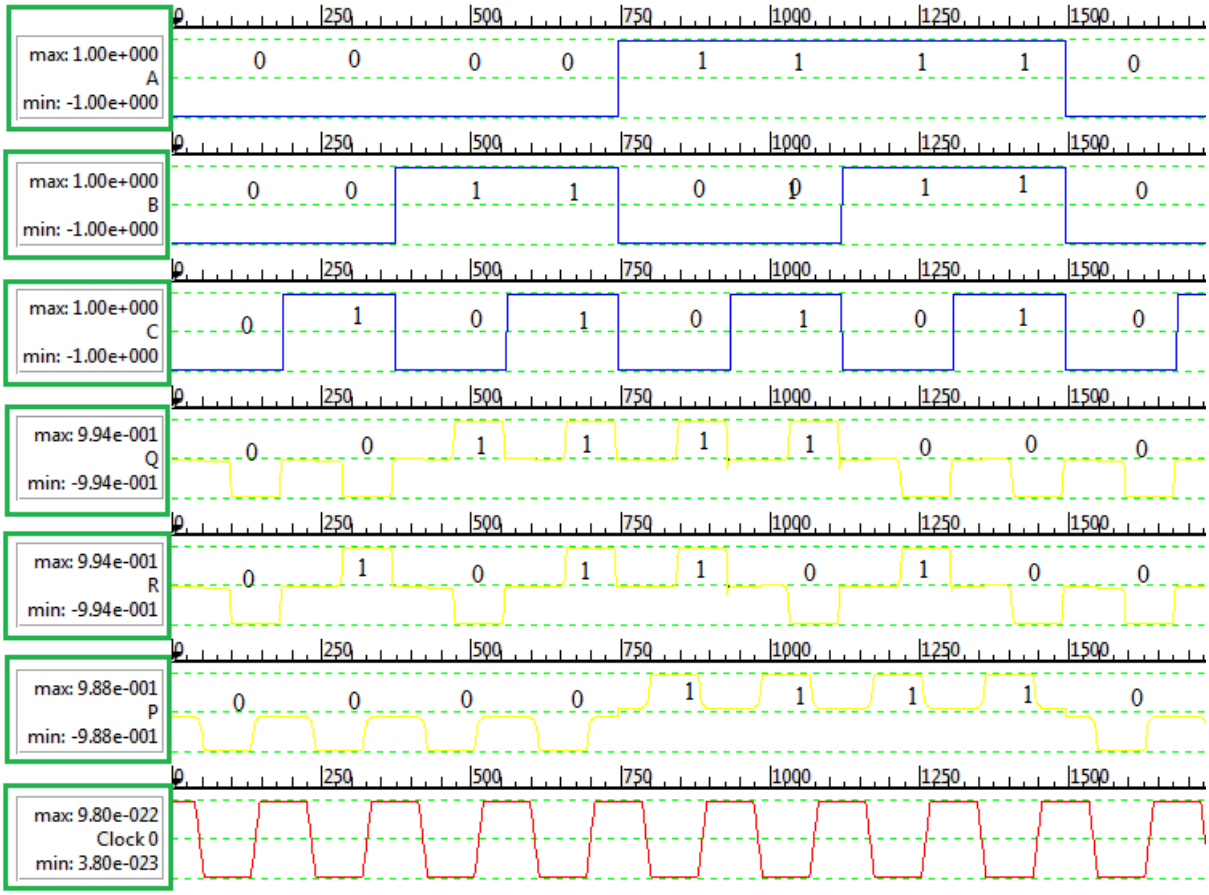

Figure 7. Simulation result of F2G.

number of QCA cells employed, the total accessible area, the clock delay, and the crossover all influence the relationship.

Table 3 demonstrates that the FG circuit designed in this article has fewer cells and a smaller system area than previous designs. Table 4 and Table 5 show the functional efficiency of the recommended structures when compared to typical RUG and UPPG designs. Circuit parameters such as cell count, delay, and area are taken into account while evaluating performance. In comparison to the past RUG and UPPG, the recommended RUG and UPPG have made significant improvements. Table 4 shows that as compared to the optimal design, the proposed RUG gate improves cell count and area by 39 % and 20 %, respectively. Table 5 shows that when compared to the optimal design, the suggested UPPG gate improves cell count and area by 68 % and 72 %, respectively.

The total number of QCA cells employed, the total accessible area, the clock delay, and the crossover all influence the relationship. Table 3 demonstrates that the FG circuit designed

Table 1. Comparison of planned F2G configuration with presented designs.

Double Feynman gate	Cell count	Area (μm²)	Delay (cycles)	Wire crossing
F2G [6]	93	0.19	0.75	Coplanar
F2G [14]	51	0.06	0.5	-
F2G [5]	53	0.05	0.5	-
Proposed F2G	31	0.04	0.5	-

Table 2. Comparison of proposed FRG structure with existing designs.

Fredkin gate	Cell count	Area (μm²)	Delay (cycles)	Wire crossing
FRG [7]	178	0.21	1	Coplanar
FRG [14]	100	0.092	0.75	-
FRG [6]	97	0.10	0.75	-
Proposed FRG	75	0.08	0.5	-

Table 3. Comparison of proposed FG structure with existing designs.

Feynman gate	Cell count	Area (μm²)	Delay (cycles)	Wire crossing
FG [7]	78	0.09	1	Coplanar
FG [8]	54	0.038	0.75	Multilayer
FG [6]	53	0.07	0.75	-
FG [9]	37	0.023	0.75	-
FG [11]	32	0.03	0.75	-
FG [14]	34	0.036	0.5	-
FG [15]	26	0.03	0.5	-
Proposed FG	13	0.02	0.5	-

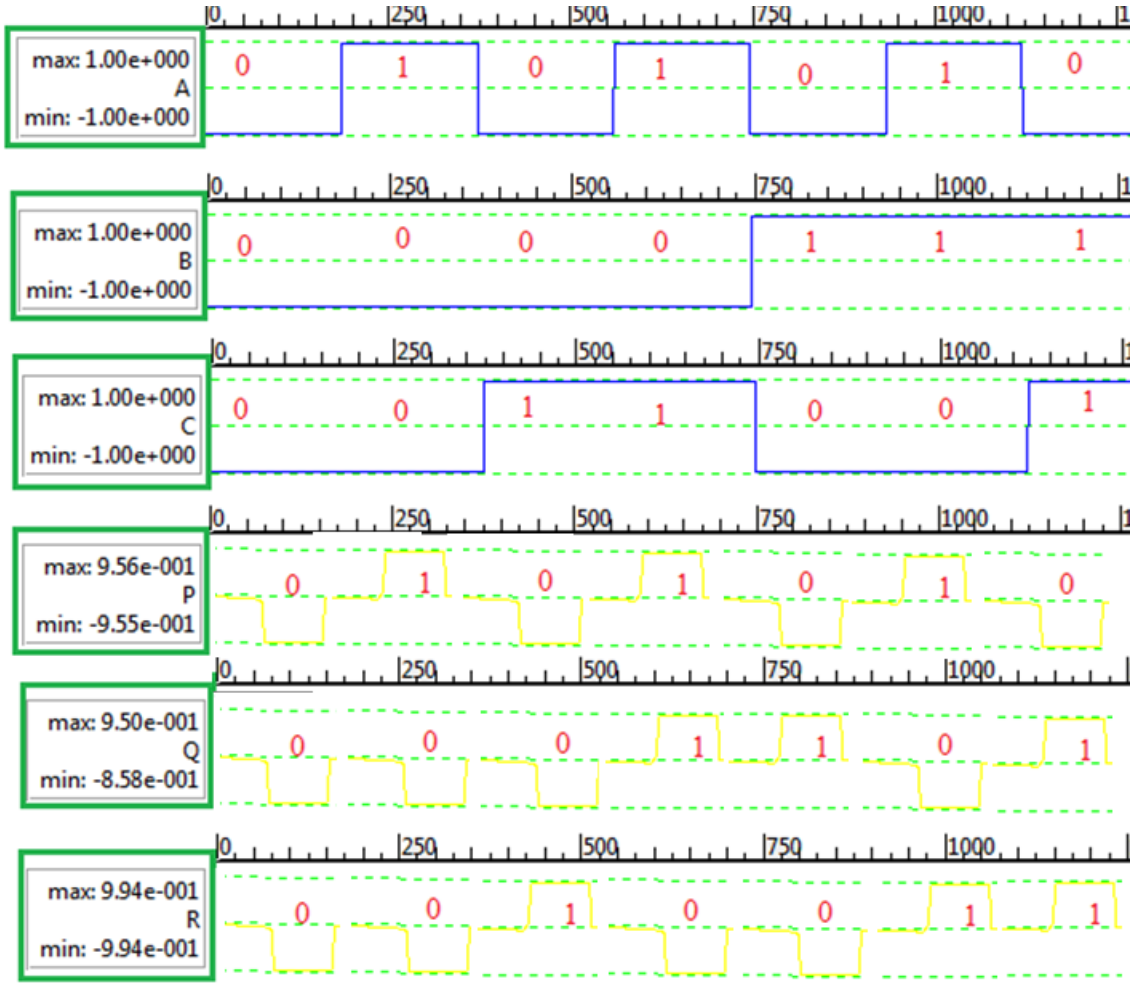

Figure 8. Simulation result of FRG.

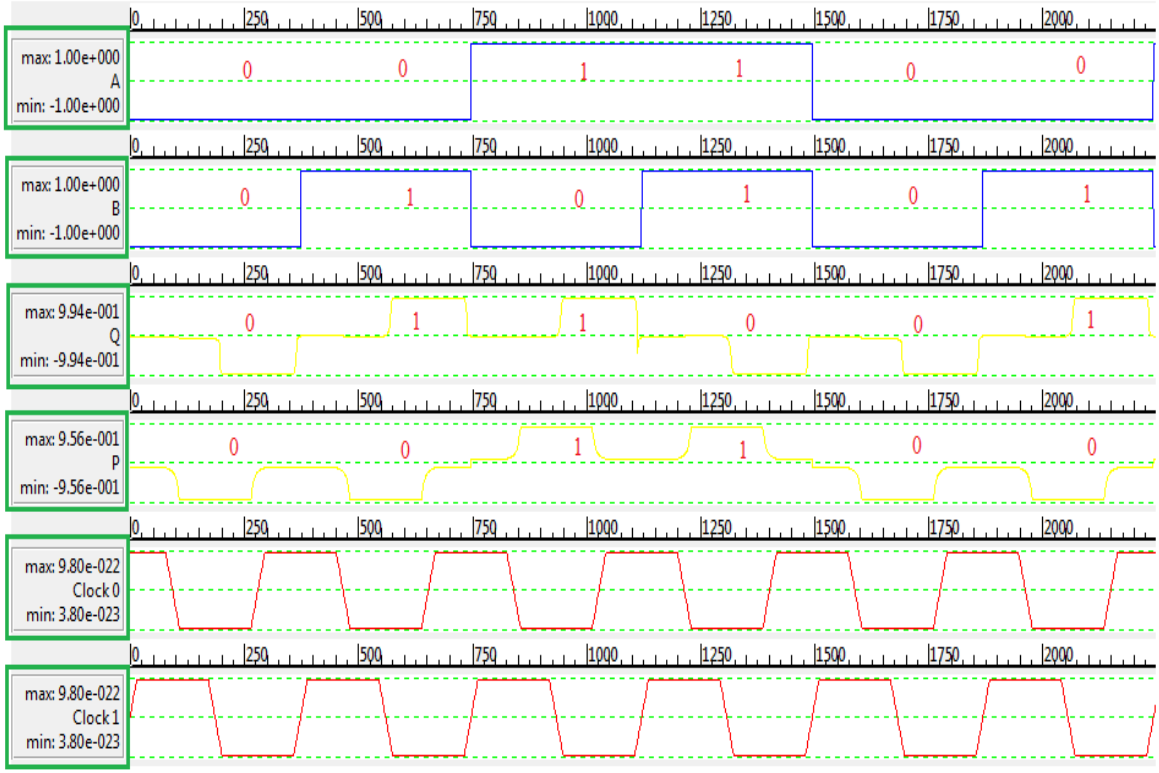

Figure 9. Simulation result of FG.

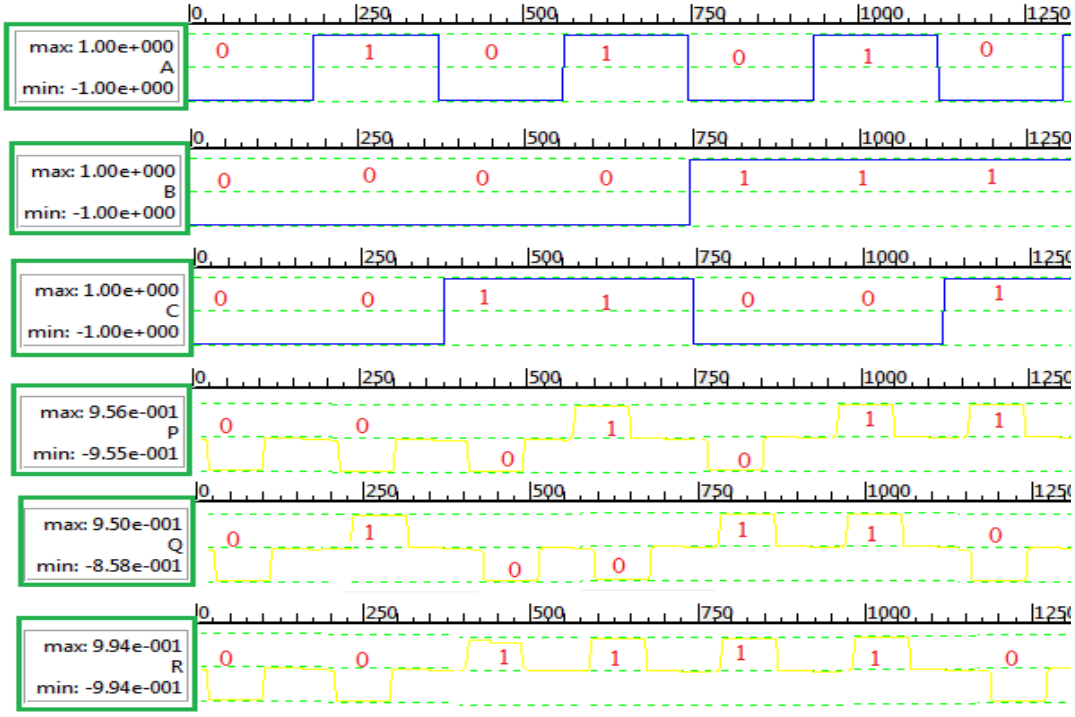

Figure 10. Simulation result of RUG.

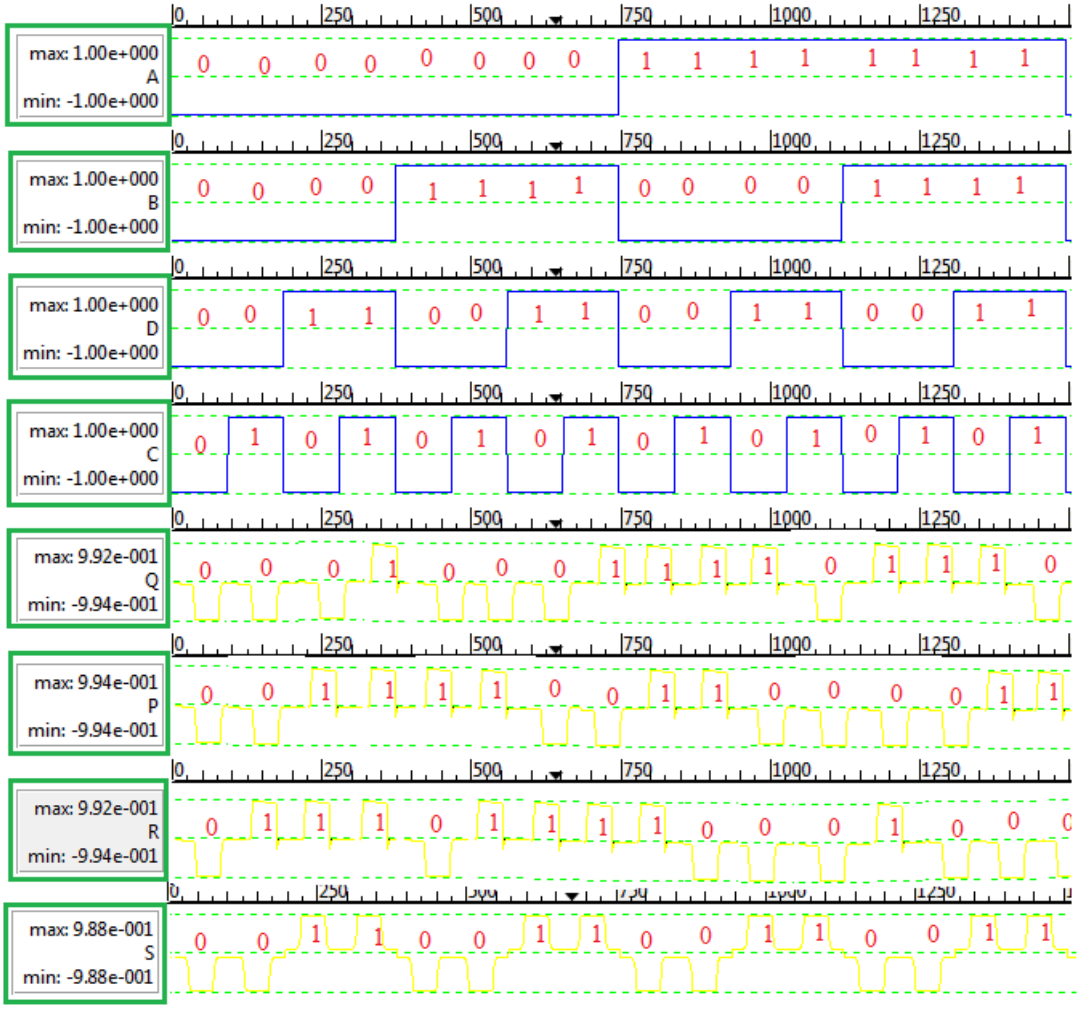

Figure 11. Simulation result of RUG.

Table 4. Comparison of proposed RUG structure with existing designs.

RUG gate	Cell count	Area (μm²)	Delay (cycles)	Wire crossing
RUG [7]	170	0.23	1	Coplanar
RUG [16]	187	0.22	1.75	Coplanar
RUG [6]	97	0.10	0.75	-
Proposed RUG	59	0.08	0.5	-

Table 5. Comparison of proposed UPPG structure with existing designs.

UPPG gate	Cell count	Area (μm²)	Delay (cycles)	Wire crossing
UPPG [17]	233	0.29	2.5	Coplanar
Proposed UPPG	75	0.08	0.5	-

Table 6. Energy dissipation of the proposed reversible logic gate structures.

Gate	Average energy dissipation per cycle (eV)	Total energy dissipation (eV)
F2G	$2.66 \cdot 10^{-3}$	$2.92 \cdot 10^{-2}$
FRG	$3.20 \cdot 10^{-3}$	$3.52 \cdot 10^{-2}$
FG	$1.69 \cdot 10^{-3}$	$1.86 \cdot 10^{-2}$
RUG	$3.55 \cdot 10^{-3}$	$3.90 \cdot 10^{-2}$
UPPG	$3.55 \cdot 10^{-3}$	$3.90 \cdot 10^{-2}$

in this article has fewer cells and a smaller system area than previous designs. Tables 4 and 5 show the functional efficiency of the recommended structures when compared to typical RUG and UPPG designs. Circuit parameters such as cell count, delay, and area are taken into account while evaluating performance. In comparison to the past RUG and UPPG, the recommended RUG and UPPG have made significant improvements. Table 4 shows that as compared to the optimal design, the proposed RUG gate improves cell count and area by 39 % and 20 %, respectively. Table 5 shows that when compared to the optimal design, the suggested UPPG gate improves cell count and area by 68 % and 72 %, respectively.

The comparison shows that the proposed structures for the existing reversible gates have a compact architecture than the existing designs. The energy dissipation analysis of the proposed gate structures is as shown in Table 6. Results show that the proposed structures outperform previous reversible gate designs and thus suitable for application toward complex nano-scale architectures in QCA.

4. CONCLUSION

In this study, the reversible gates like Feynman gate (FG), double Feynman gate (F2G), reversible universal gate (RUG), Fredkin gate (FRG), and universal parity preserving gate (UPPG) are designed using QCA technology with optimum area. The designed layouts of the reversible gates have zero wire crossings. The simulation results have been verified using QCA designer software. The suggested F2G, FRG, FG, RUG and UPPG QCA layouts are designed only with 31, 75, 13, 59 and 75 QCA cell count and 0.04 μm², 0.08 μm², 0.02 μm², 0.08 μm², and 0.08 μm² area respectively. Then, we measured and compared the robustness of the recommended reversible gates to the existing gates using standard metrics. The simulation results show that the suggested reversible gates perform better in terms of cell count and area by 42 %, 23 %, 50 %, 39 %, and 68 % and 31 %, 20 %, 33 %, 20 %, and 72 %, respectively. The suggested architectures outperform existing reversible gate designs, indicating that they are better suited for usage in QCA in complicated nanoscale systems.

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