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Method of integral nonlinearity testing and correction of multi-range ADC by direct measurement of output voltages of multi-resistors divider

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ABSTRACT
A method of testing points generation for the identification and correction of the integral nonlinearity of high performance ADC's is presented. The proposed method is based on averaging all voltages of the multi-resistor voltage divider. The influence of the resistors errors and random errors of the ADC on the residual error of the integral nonlinearity correction for method based on multi-resistor divider is investigated.

Section: RESEARCH PAPER

Keywords: Integral Nonlinearity; Multi-Resistor Voltage Divider; Residual Error

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1. INTRODUCTION

The application of digital signal processing algorithms and computer systems in all fields of our life results in the implementation of analogue-to-digital converters (ADC) as a component of modern measurement systems. In some cases the ADC's metrology parameters determine the characteristics of the whole measurement system. Particularly, this point is important for measurement systems of electrical quantities. Therefore improving the ADC is an essential task for higher measurement accuracy.

The market of precision DC ADC's is led by converters based on sigma-delta modulators SDM [1], [2]. The high accuracy of these components is provided by the implementation of null setting and calibration. These methods provide decrease of additive and multiplicative conversion errors. Therefore, the conversion error is composed of the following errors: calibration voltage source, multiplexer and residual ADC errors. The most significant component of the residual ADC error is its integral nonlinearity. For example, the maximum allowable integral nonlinearity of the 24-bit ADC AD7714 [3] is 15 ppm. This nonlinearity corresponds to the 16th bit, that is approximately 8 least significant bits (LSB) are *a priori* inaccurate and excessive. Therefore, for this ADC, to obtain a higher accuracy than 15 ppm the integral nonlinearity should be corrected. In the same case, the noise level of this ADC does not exceed 2.5 LSB. Therefore, the ADC has approximately 5.5 stable bits, and therefore it cannot be used when high accuracy is required. Moreover, the accuracy of measurement results obtained by the implementation of the substitution method [4] in an ADC is defined by the ADC's integral nonlinearity [5]. So correction of the ADC's integral nonlinearity provides a higher accuracy of the measurement results. In [6] a method for the identification of the ADC's integral nonlinearity in the set of testing points conventionally called as basic method was proposed. This method provides the generation of a set of testing points, which correspond to the number sequence $(1/N)U_R$ where U_R is the range of the ADC and N an integer. This means that all testing points are grouped

in the lower half of the ADC's range. The main objective of this work is to develop and investigate the method of ADC's integral nonlinearity identification and correction with a uniform distribution of the testing points over the range.

2. APPROACH OF TESTING POINTS GENERATION

The proposed method of testing points generation is based on analog to digital conversion of the output signals of the voltage divider consisting of N serially combined resistors $R_1, R_2, ..., R_N$, connected to the reference voltage source U_{REF}. The measurement circuit is shown in Figure 1.

According to Kirchhoff's voltage law, we have the following equation

$$U_{REF} = \sum_{i=1}^{N} U_{Ri} \tag{1}$$

where U_{Ri}, $i = \overline{1,N}$ is the voltage of the appropriate resistors of the divider.

The average voltage of all resistors of the divider $\overline{U}$ can be computed as:

$$\overline{U} = \frac{1}{N}\sum_{i=1}^{N} U_{Ri} \tag{2}$$

Taking into account (1), (2) can be presented as

$$\overline{U} = \frac{U_{REF}}{N} \tag{3}$$

It means that the average voltage of all resistors of the divider $\overline{U}$ does not depend on the voltages of the separate resistors. In addition, according to Ohm's law, the resistances of these resistors do not influence the average voltage.

So, we have an indirect measurement described by the function $y = h(x)$, where $y \equiv \overline{U}$, $x \equiv U_{REF}$ $h(x) \equiv \frac{x}{N}$.

Therefore, the absolute measurement error Δy is [7]:

$$\Delta y = h'(x) \cdot \Delta x \tag{4}$$

where $h'(x)$ is the derivative of the function $h(x)$ and Δx the absolute error of the argument.

Taking into account that N is a natural number, (4) can be converted to

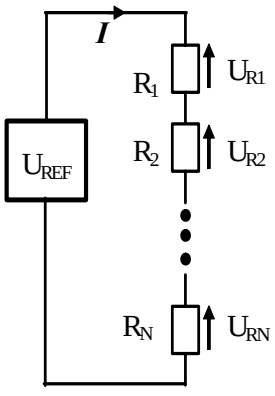

Figure 1. Circuit of N -resistors voltage divider.

$$\Delta_{\overline{U}} = \frac{\Delta_{U_{REF}}}{N} \tag{5}$$

where $\Delta_{\overline{U}}$ is the absolute error of the average voltage $\overline{U}$ and $\Delta_{U_{REF}}$ the absolute error of the voltage source U_{REF}.

The relative error of the average voltage $\overline{U}$ – $\delta_{\overline{U}}$ is

$$\delta_{\overline{U}} = \frac{\Delta_{\overline{U}}}{\overline{U}}100\,\% = \frac{\frac{\Delta_{U_{REF}}}{N}}{\frac{U_{REF}}{N}}100\,\% = \frac{\Delta_{U_{REF}}}{U_{REF}}100\,\% = \delta_{U_{REF}} \tag{6}$$

with $\delta_{U_{REF}}$ the relative error of the voltage source U_{REF}.

Taking into account (6), the next intermediate conclusion can be made: the error caused by the measurement converter based on a multi-resistor voltage divider with averaging voltages of all resistors tends to zero. It provides the opportunity of generating the set of testing signals for the ADC with an exactly predefined ratio.

In case of ADC calibration by the voltage source of the divider U_{REF}, the average voltage $\overline{U}$ as testing point for the identification of the ADC's integral nonlinearity can be used.

The result of analog to digital conversion (C) of an input voltage U [8] is:

$$C = C_0 + \frac{C_{REF} - C_0}{U_{REF}}U + f(U) \tag{7}$$

where:

C_0 – result of analog to digital conversion by the null setting channel;

C_{REF} – result of analog to digital conversion by the calibration channel (for input connected to voltage U_{REF});

$f(U)$ – integral nonlinearity of ADC's conversion function, and for $f(U_{REF}) = f(0) = 0$.

Taking into account (7), and using (2) and (3) results in

$$\frac{1}{N}\sum_{i=1}^{N}\frac{C_i - C_0 - f(U_i)}{C_{REF} - C_0}U_{REF} = \frac{1}{N}U_{REF} \tag{8}$$

where C_i is the result of analog-to-digital conversion of the voltage U_{Ri}.

After simplifying (8) we get

$$\sum_{i=1}^{N}(C_i - C_0 - f(U_i)) = C_{REF} - C_0 \tag{9}$$

The average voltage of the nonlinear component of the conversion function for all voltages generated by the multi-resistor divider $\overline{f(U)}$ can be computed as

$$\overline{f(U)} = \frac{1}{N}\sum_{i=1}^{N} f(U_i) \tag{10}$$

Taking into consideration (10), (9) can be transformed as

$$\overline{f(U)} = \frac{1}{N}\left(\sum_{i=1}^{N}(C_i - C_0) - (C_{REF} - C_0)\right) \tag{11}$$

The value of $\overline{f(U)}$ is computed using the value of the integral nonlinearity at the testing point $\overline{U} = U_{REF}/N$.

An analysis of the influence of the tested ADC on the residual error [6] shows the potential of this implementation method for an ADC with a smooth conversion characteristic.

So, it is shown that the multi-resistors voltage divider provides precision identification of the ADC's integral nonlinearity in one testing point without using precision components. The proposed method is called a basic method [6] and it provides increasing the number of generated testing points by choosing N. Since N contains the set of natural divisors $\{m_1,\dots,m_t\}$, it is the set of natural numbers $\{k_1,\dots,k_t\}$ which satisfies the condition $N = m_i \times k_i;\ i=\overline{1,t}$. It allows the conversion of voltages on the cascades of k_i $\left(i=\overline{1,t}\right)$ serially connected resistors, which corresponds to (1). Therefore, the integral nonlinearity of the ADC can be computed in accordance to the set of t voltages:

$$\overline{U}_i = \frac{U_{REF}}{N} k_i = \frac{U_{REF}}{m_i};\quad i=\overline{1,t} \tag{12}$$

The error of all these voltages corresponds to (6), and only one reference voltage source can be used.

3. PROPOSED METHOD OF GENERATING TESTING POINTS

The analysis of testing results of the basic method of identification and correction of the ADC's integral nonlinearity [6] showed a linear dependence of the residual conversion error of the density of testing points concentration. It allows us to separate at least two subranges: lower and higher half of the ADC's range, which has different residual errors after nonlinearity correction using the basic method. The residual nonlinearity error of the upper subrange is approximately one order higher than the residual nonlinearity error of the lower subrange. Taking into account these results we propose to generate testing points for nonlinearity identification of a multi-range ADC (in the simplest case for a double range ADC) as the voltages of the serially connected resistors of the multi-resistor voltage divider, measured using the lower subrange of the highest range and to use these voltages for calibration and nonlinearity identification/correction for all other ranges. In the case of a voltage divider with N resistors ($R_1, R_2, ..., R_N$), the following testing points are generated: the first is the voltage on resistor R_1, the second is the voltage on the serially connected resistors R_1 and R_2, the third for $R_1...R_3$, etc. up to the $N/2$-th: $R_1...R_{N/2}$. In general, this approach provides the generation of $N/2$ testing points with relative high precision uniformly distributed in the lower half of the highest range of the ADC. Calibration and nonlinearity identification of the lower ranges provide high accuracy and a uniform distribution (in the case when the ratio of higher range to lower range is not less then two) of all generated testing points. Besides, it is possible to generate an arbitrary number of testing points by selecting an appropriate N and increasing the generated testing points with a smaller increase of N in comparison with the basic method.

4. INVESTIGATION OF THE RESIDUAL ERROR

Investigation of the residual nonlinear error by experiments demands high precision equipment with errors 3…5 times less then the expected residual nonlinearity, and corresponding to 0.5 ppm. Besides, it is necessary to have the opportunity to set the level and the form of the ADC's nonlinearity with the same error level. Therefore, the aim is to investigate the proposed method by simulation and to evaluate the influence of resistor errors and ADC noise on the residual nonlinear error for various nonlinear functions. Generally, the method of investigation results in emulation of the integral nonlinearity by a set of curves and its computing according to the proposed method. The difference between emulated and computed curves is the error for analysis. The algorithm for this investigation consists of the following steps:

- definition, by random way, of two curves, which simulate the ADC's nonlinearities in the higher and lower ranges;
- definition of resistance of the divider's resistors $R_1, R_2, ..., R_N$ with random deviation from the average value for simulation of the resistors' error;
- computation of the results of the analog to digital conversion for appropriate combinations of resistors for the implementation of the basic method for ADC's higher range nonlinearity identification;
- noising of these conversion results to simulate the random error of the ADC;
- computation of parameters of the correction function for the ADC's higher range nonlinearity;
- computation of voltages on the serially connected resistors $R_1;\ R_1, R_2;\ R_1...R_3;\ ...\ ;R_1...R_{N/2}$ using simulated results of the analog-to-digital conversion for these voltages in the higher range and correction of the ADC's nonlinearity in that range;
- computation of the results of the analog-to-digital conversion for these voltages using the lower range of the ADC;
- noising these conversion results for simulation of the random error;
- computation of parameters for the correction function for the lower range nonlinearity;
- computation of the residual error of the integral nonlinearity correction for the lower range as the difference between the defined curve and the computed correction function for this range.

So, accumulating the set of residual error curves we can implement the statistical data manipulation methods for investigation of parameters of the proposed method and their sensitivity to the ADC's random error and resistors error. The nonlinearity simulation curves for the higher and lower ranges are based on the fourth order polynomial functions with random coefficients [6]. The validity criterion of each curve is not exceeding by the absolute maximum value on the range of the ADC of the 250 quantums. This constant corresponds to the maximum allowable nonlinearity of the AD7714. Examples of such curves are presented in Figure 2, with nonlinearity in quantum along the Y-axis, and the input voltage in percents of the range along the X-axis. Also, two curves with maximum and minimum values for 500 curves generated for our investigation are presented.

The software verification was done by setting "ideal" resistors and ADC (zero error of all resistors and zero ADC's random error). In this case we obtained a maximum error of 0.05 quantum, which we can explain by error rounding during computation. Therefore, we can expect that the developed

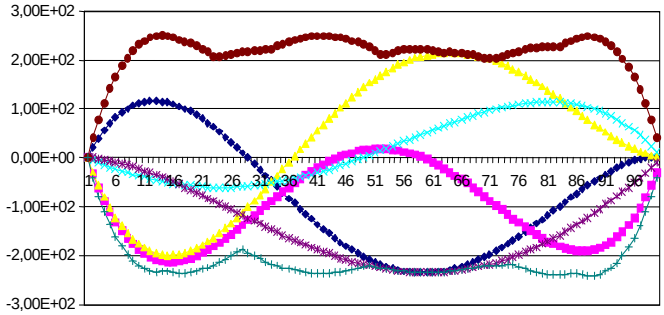

Figure 2. Simulated nonlinearity of the ADC.

models and software are adequate and can be used for investigation of the influence of component errors on the residual error after integral nonlinearity correction.

The simulation was done for a 12-resistors voltage divider. This number of resistors was selected based on two contradictory requirements:

– maximum number of natural dividers for implementation of the large amount of generated testing points (number 12 totally has six dividers: 1, 2, 3, 4, 6, 12);
– minimum number of resistors for decreasing of their channels of multiplexer and simplification (a 12-resistors divider demands 2 switches with 13 channels for the multiplexer).

The simulated resistors' error is ±1 and ±2 %. It corresponds to 10 … 20 years of exploitation of widely used wire-wound-type resistors with allowable error ±0.1 %. The curves of residual error vs input voltage for the lower range in the case of resistor error ±1 % is presented in Figure . The five randomly selected curves and two curves with maximum and minimum values for 500 curves are presented. As we can see, the maximum value does not exceed 1.5 quantum in the worst case. This value is comparable with the ADC's resolution. The maximum residual error for resistors with error ±2 % does not exceed 3.5 quantums. This value is comparable with the ADC noise.

The results testified the residual error for a noise level of ± 6 quantums. They are presented in Figure 4. There are five randomly selected curves and two curves with maximum and minimum values for 500 curves. As we can see, the maximum value does not exceed 18 quantums in the worst case. Generally, these results are close to the results of the basic method investigation [6] but they correspond to the whole lower range of the ADC instead of the lower subrange for the basic method. The form of the curves obtained for other noise levels of the ADC is similar to the curves presented in Figure 4.

Figure 5 shows the dependence of the maximum value of the residual error for the lower range versus the noise level.

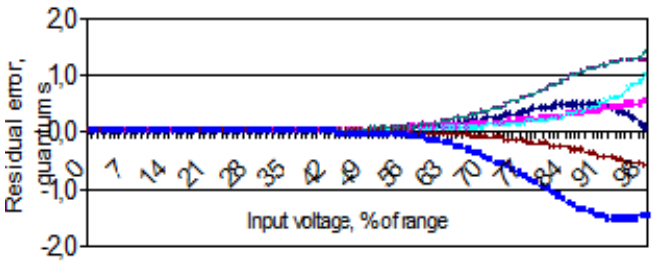

Figure 3 Residual error vs input voltage for resistors' error ± 1 %.

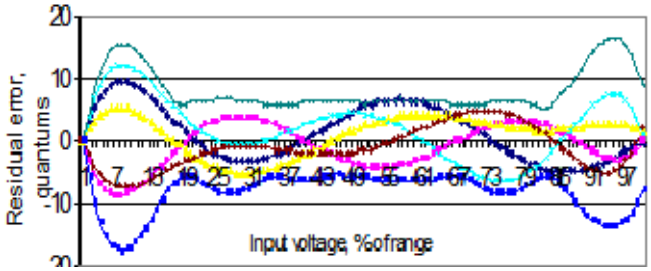

Figure 4. Residual error vs input voltage for ADC noise ± 6 quantums.

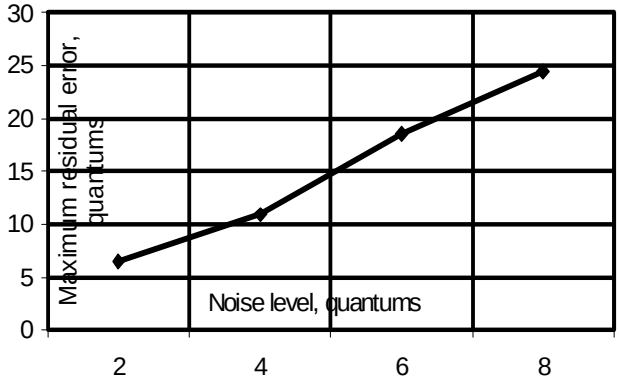

Figure 5. Maximum residual error vs ADC noise level.

Taking into consideration the linear character of this dependence, we can conclude that the noise influence coefficient for the presented method does not exceed three for a 12-resistors voltage divider.

5. CONCLUSIONS

The investigation of the proposed method of integral nonlinearity identification and correction for the lower range of the ADC leads to the following conclusions:

– the number of generated testing points depends on the number of resistors in the voltage divider and all of them are evenly distributed over the range. It provides the generation of testing points corresponding to the requirements of the actual standard for metrology verification of ADCs with a smooth conversion characteristic [9];
– the influence of resistor errors of the voltage divider on the residual error is comparable with the ADC's resolution and it is negligible in comparison with other errors;
– the influence of the ADC's random error on the residual error is dominating and proportional to its noise level with proportionality factor three for a 12-resistors voltage divider.

The weak sensitivity of the proposed method to resistor errors and ADC noise provides the opportunity of its implementation for metrological verification subsystem [10] of ADCs using a single channel reference voltage source. The error of such metrological verification is mainly defined by the error of the implemented reference voltage source, therefore, metrology support of such metrological verification subsystem is reduced to the verification of the reference voltage source. It provides the opportunity to embed this metrological verification subsystem with reference voltage source into the ADC.

Implementation of proposed method demands special hardware and software. This hardware consists of multi-resistors divider, multiplexer and controller. The most complex operation of software is computing of polynomial function with rational coefficients and integer argument. Therefore it can be implemented on microcontroller of ADC or external data processing module. Using external data processing module and external hardware provides implementation of metrological verification subsystem without accessing to ADC's hardware or software. Example of universal data processing module, which corresponds to requirements of proposed method, is presented in [11]. It is compatible with wide set of serial peripheral interfaces for connection ADC and mentioned hardware. Its computing power is enough for implementation proposed method in real time.

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