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DSP based data acquisition system with on-board processing

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Abstract-This paper presents the development, implementation and characterization of a data acquisition system with the capability of on-board processing the acquired data. The system features 4 differential channels, with simultaneous acquisition and a maximum sampling rate of 600 kS/s. The ADSP-21489 digital signal processor is selected to control the system and act as the central processing unit. The interface between the system and a personal computer is performed through USB Hi-speed protocol.

I. Introduction

The need to control, monitor and measure complex systems is essential in different areas [1,2]. The main goal of acquisition systems is to measure electrical or physical phenomena and make it available in the digital domain [3]. By processing the measured data it is possible to get valuable information and take eventual correcting actions. While most of the systems used today are designed for specific tasks, the popularity of portable multi-purpose modules has increased. These present a more versatile solution, since they can be easily adapted to numerous applications with good versatility and reduced cost. These modules typically include multiple channels, a good diversity of input ranges, good resolution analog to digital converters, medium sampling rates (up to 1 MS/s) and in some cases, digital I/O ports, digital to analog channels and digital counters.
The goal of this work is to develop, implement and characterize a 16-bit four-channel multi-range simultaneous data acquisition system with on-board signal processing capabilities. To achieve this goal, a digital signal processor is used to control the entire system and perform the on-board processing. The system has to be able to execute simultaneous acquisitions at a maximum rate of 600 kS/s and have an analog bandwidth of 1 MHz. In the most used architecture for simultaneous multi-channel acquisition systems, each channel has its own dedicated circuitry and analog to digital converters. Multiple and independent voltage ranges must be available to allow accurate measurement of signals with different dynamic ranges. The input channels are acquired differentially with impedance at low frequencies of 1 MΩ (single-ended) and 2 MΩ (for differential acquisitions) and must withstand a considerable level of incorrect usage (i.e., incorrect direct connection to the power grid) without damaging the system circuitry and still ensure operability (i.e., no fuses).

II. System architecture

Generically, a data acquisition system can be divided in three blocks. In the first block, the signal conditioning circuit adapts the input signal before digitalization. This includes attenuation or amplification to account for different input ranges. An important function of the conditioning circuit is to protect the system against non-ideal conditions, like overload, incorrect usage or electrostatic discharge (ESD). In the second block, after the conditioning circuit, the analog to digital converter (ADC) digitalizes the signal. In the third block, to control the system a microcontroller is used (PIC - Peripheral Interface Controller [4], DSP - Digital Signal Processor [2] or FPGA - Field Programmable Gate Array [3], [1]). This device is responsible for the configuration of the channels, by programming the amplifiers' gain, controlling the sampling frequency, collecting and transferring the sampled data. In some cases, the system has the ability to process data and control other systems, like actuators for example. In the system described in this paper, the control unit must be able to perform on-board processing such as FFT calculation for example.
In Figure 1, the proposed system architecture is shown. The system has four identical input analog channels, with independent gain setting and offset compensation, and individual ADCs. In addition to the described modules, the system has a 16 Mbit flash module to store the DSP program which is loaded upon reset or booting. A DSP external memory module was added to increase storage capacity and further increase flexibility in the processing of large amounts of data. The SDRAM has 256 Mb capacity in 16-bit words. USB 2.0 Hi-speed is used in the communication with an external computer. Implementation is done using a FT2232H device.

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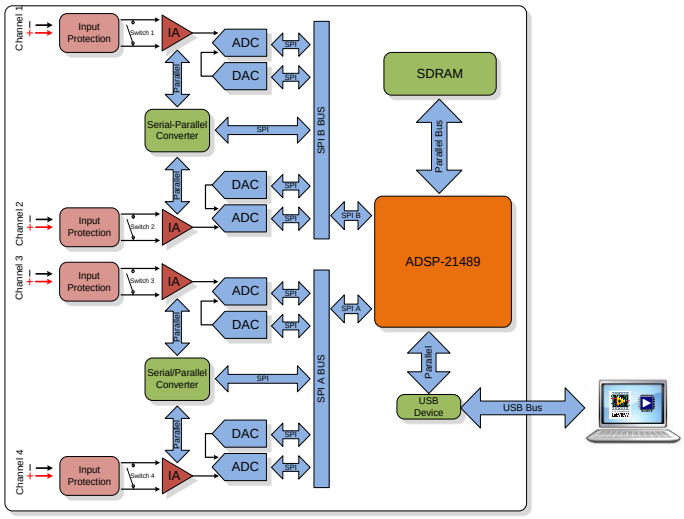

Figure 1. System architecture.

The input attenuation/protection circuit is shown in Figure 2. Its purpose is to attenuate the input signals 5 times and to protect the amplifiers, the ADCs and the DSP from incorrect usage [5]. It is dimensioned to sustain input direct connection into the power grid without any system damage and complete operability afterwards. The set R2, R3, C_{var} and the equivalent input capacitance from R3 onward, form the basis of a compensated attenuator as is traditional for instance in oscilloscopes. R1 and R4 are included to ensure that during transient connection, and while these capacitors are discharged, the maximum current in the protection schottky diodes (D1) do not cause their failure. The diodes are included to protect over voltages from reaching the programmable amplifiers.

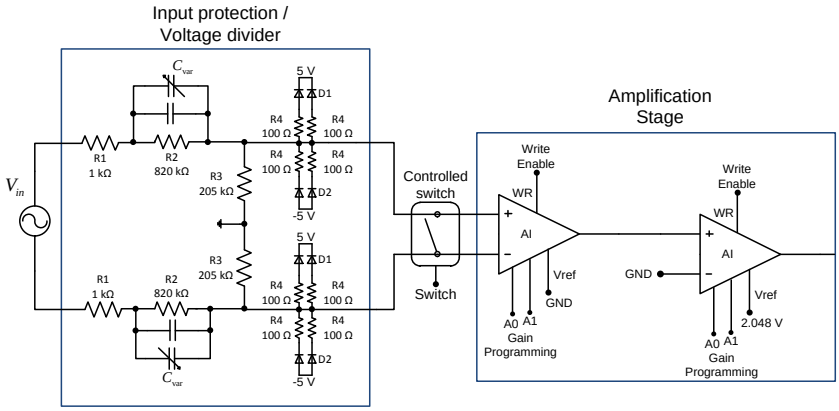

Figure 2. Analog signal conditioning circuit.

Although the inclusion of R1 makes the voltage divider uncompensated (as shown in the equivalent circuit of Figure 3), its value was dimensioned so that the extra pole (located at 10 MHz) and extra zero (located at 796 MHz) are at frequencies well above the target input analog bandwidth (1 MHz).

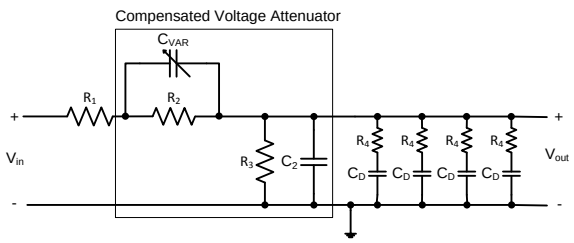

Figure 3. Equivalent analog input circuitry for single-ended acquisitions. C2 is from the AI input capacitance and the controlled switch for offset adjustment.

Two instrumentation amplifiers (IA) are used in each channel. The gain combinations from the two amplifiers enable the implementation of the nine input ranges ±0.1 V, ±0.2 V, ±0.4 V, ±0.5 V, ±1 V, ±2 V, ±2.5 V, ±5 V and ±10 V. Each of the IA are AD8250 with programmable gains for 1, 2, 5 and 10, slew-rate of 20 V/µs and CMRR of 80 dB. The definition of the gain is set by the DSP using a SPI connection and a serial/parallel converter (one for each channel pair) as shown in Figure 4 and as it is directly related with the input range desired by the user, it is set before acquisition starts. Three bits are used for each IA (two for the gain bits and one for the write enable).

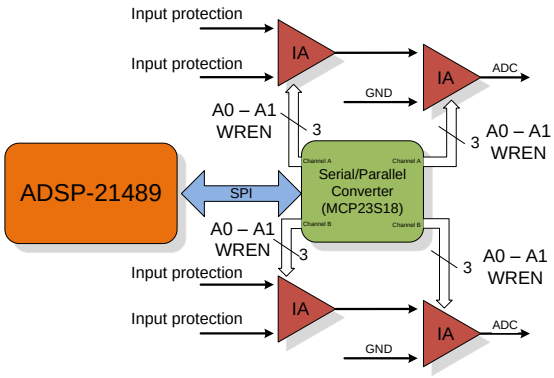

Figure 4. Detail of gain programming stage. Since the gain changes are only done before acquisition starts, and in order to reduce connections to the DSP and save on SPI ports, only serial parallel converter is used and it shares the same SPI for each channel pair.

The selected ADCs are 16-bit SAR with maximum sampling rate of 1 MS/s, unipolar input voltage, SPI interface but with the ability of use in daisy-chain configuration (as shown in Figure 5) to share the same SPI connection. The ADC range is set to [0 ; 4.096] V and the Vref input of the final IA (see Figure 2) is used to add the DC component necessary to ensure a unipolar signal at the ADC inputs.

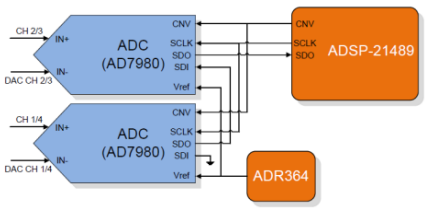

Figure 5. ADC daisy-chain connection Each pair of ADCs shares the same SPI connection to the DSP.

The final prototype is presented in Figure 6.

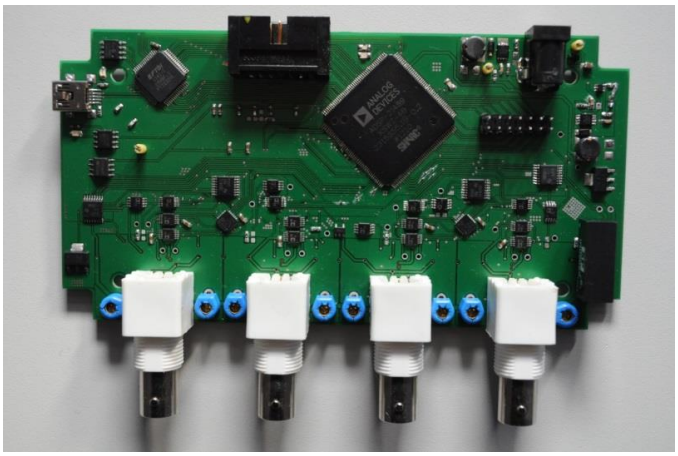

Figure 6. Implemented system. The final PCB has 145 mm length and 75 mm width.

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III. System characterization

The frequency response was measured with a TTi TG1010A function generator controlled with IEEE 488.2 and an application developed in LabVIEW to control the function generator, retrieve the DAQ samples and process the results. The final results for one of the input channels and for all the input ranges are shown in Figure 7. It can be seen that the overall input channel bandwidth is limited by the response of the lowest range and corresponds to 2.3 MHz. However, noticeable distortion was measured starting at 1.6 MHz due to the slew-rate of the amplifiers.

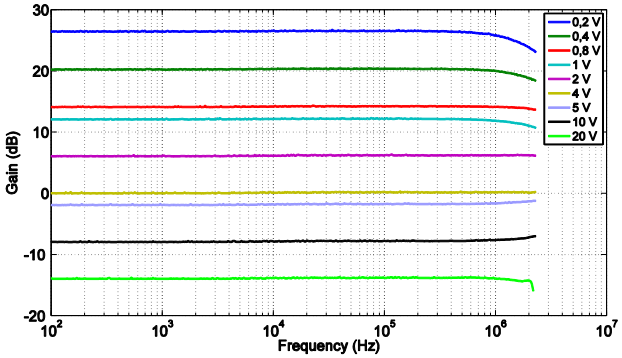

Figure 7. Input frequency responses for all ranges in one channel.

The delay/rising time response of one of the channels was measured with a TDS5034 oscilloscope and the results are depicted in Figure 8. The rise time is 57.4 ns while the delay is 112 ns.

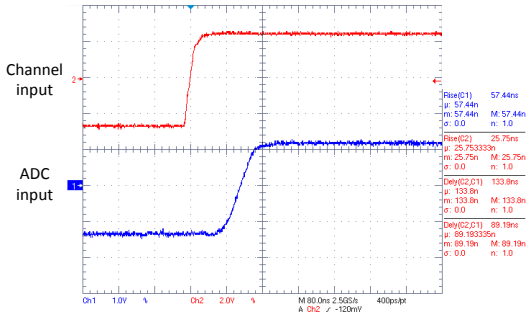

Figure 8. Delay/rising time measurement.

In Figure 9, the results from one of the cross-talk measurements are presented. The stimulus signal is a 100 kHz sinusoidal signal. Typical cross-talks of around -80 dB were achieved.

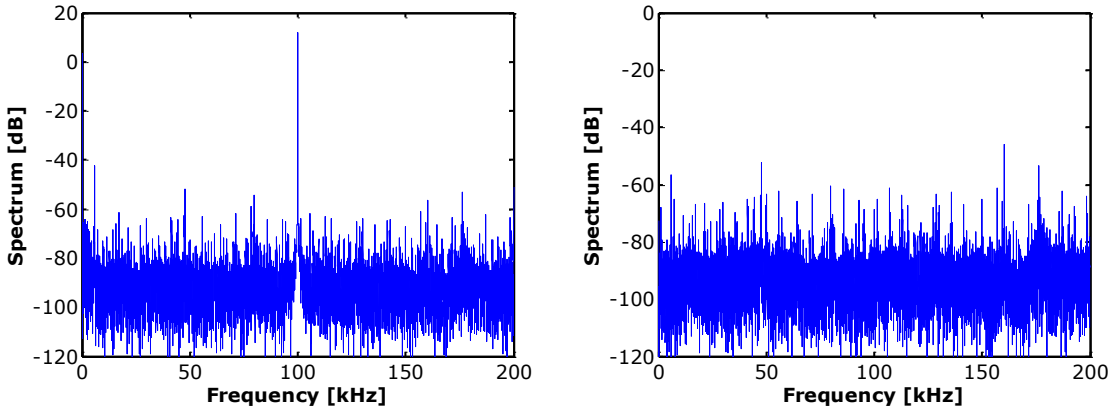

Figure 9. Cross-talk measurements for 100 kHz. The spectrum on the left side represents the input sinusoidal signal while the spectrum on the right side is the one obtained on the non-stimulated channel.

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IV. Measurement Results

To demonstrate the simultaneous acquisition of the developed DAQ, a 10 kHz sinusoidal signal was applied to all channels as they were acquired with a sampling rate of 400 kS/s. In Figure 10, two of the channels are depicted. In this case, the delay estimated using the seven-parameter sine-fitting algorithm [6], is under 125 ns.

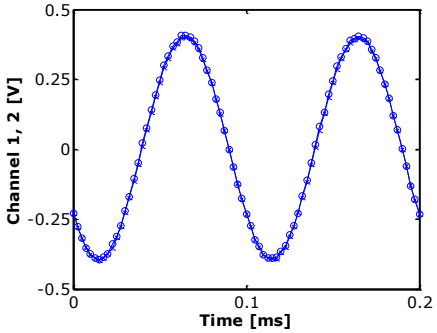

Figure 10. Simultaneous acquisition of a 10 kHz signal. Both channels are represented (channel 1 are the circles and channel 2 are the crosses).

In Figure 11 one example of an acquisition, as shown in the front panel of the developed LabVIEW interface application, is shown. The application enables the selection of the channels to be acquired, their independent ranges, the number of samples and the sampling rate.

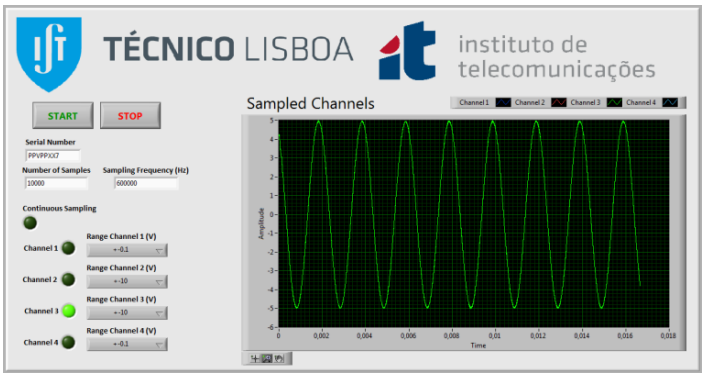

Figure 11. Front panel of one acquisition example.

In Figure 12, the amplitude of the FFT calculated within the device is shown. The input signal corresponds to a sinusoidal or triangular sinal with 1 kHz and amplitude of 0.4 V sampled at 40 kS/s with 65536 samples.

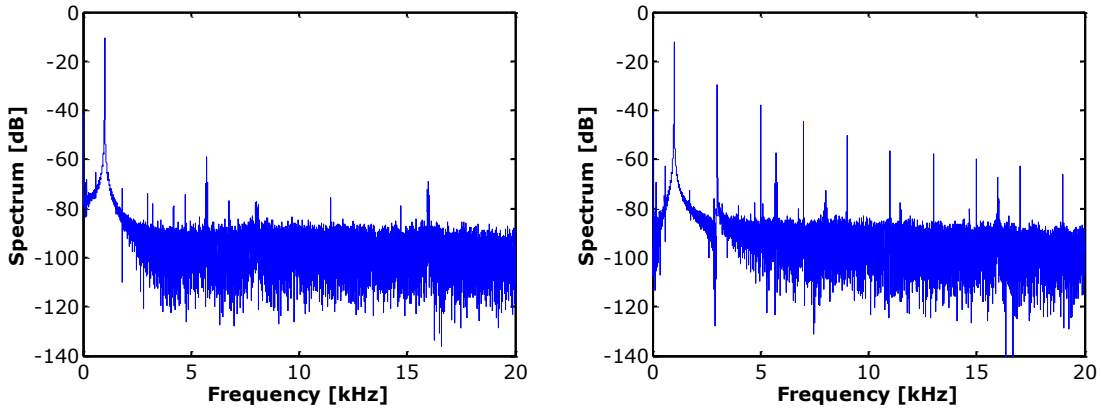

Figure 12. Example of FFT calculation done within the data acquisition device. Sinusoidal signal (left) and triangular signal (right)

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V. Conclusions

The development, implementation and characterization of a simultaneous data acquisition system with four-channels, multiple independent ranges, analog bandwidth of at least 1 MHz, sampling rate up to 600 kS/s and advanced on-board processing capabilities was presented. Results demonstrating the developed system characterization and performance were presented.

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